Phase-Noise Cancellation Design Tradeoffs in Delta–Sigma Fractional-N PLLs

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***Abstract*—A theoretical analysis of a recently proposed phase-noise cancellation technique that relaxes the fundamental tradeoff between phase noise and bandwidth in $\Delta\Sigma$ fractional-N phased-locked loops (PLLs) is presented. The limits imposed by circuit errors and PLL dynamics on the phase noise and loop bandwidth that can be achieved by PLLs incorporating the technique are quantified. Design guidelines are derived that enable customization of the technique in terms of PLL target specifications.**

***Index Terms*—Delta–sigma modulator, fractional-N PLL, phased-locked loop (PLL), segmented digital-to-analog converter (DAC), synthesizer.**

I. Introduction

A PHASE-NOISE cancellation technique is presented in [1] that employs a digital-to-analog converter (DAC) cancellation path to suppress the phase noise arising from quantization error in a delta-sigma ($\Delta\Sigma$) fractional-N phase-locked loop (PLL). The technique has been shown to allow a ten-fold increase in the PLL bandwidth without increasing the spot phase-noise arising from $\Delta\Sigma$ modulator quantization error for a specific PLL architecture and application: a 2.4-GHz second-order $\Delta\Sigma$ fractional-N PLL with a 460-kHz minimum bandwidth and 1-Mb/s in-loop frequency shift keying FSK modulation for a Bluetooth wireless local-area network compliant direct conversion transceiver. This paper presents a theoretical analysis of the phase-noise cancellation technique with the goal of facilitating its application to realize other wide bandwidth, low-noise $\Delta\Sigma$ fractional-N PLLs.

Circuit errors and the dynamics of the PLL impose limits on the phase noise and bandwidth achievable using the phase-noise cancellation technique. The technique employs quantization noise shaping, mismatch noise shaping, and 1-b dithering to significantly reduce these limits compared to prior art [2]–[6]. The paper quantifies the effects of noise shaping and dithering on the PLL phase noise, presents guidelines to customize the phase-noise cancellation technique as a function of the PLL target specifications, and presents guidelines to reduce the hardware complexity of the technique without adversely effecting the PLL phase noise.

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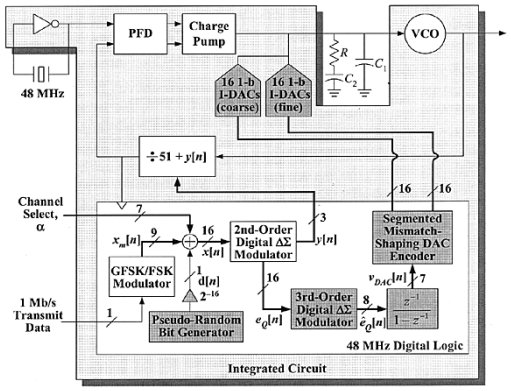

Fig. 1. A high-level functional diagram of the $\Delta\Sigma$ fractional-N PLL presented in [1].

Section II presents an overview of the phase-noise cancellation technique and describes the various ways in which it can be customized. Sections III and IV analyze the limits imposed on the effectiveness of the phase-noise cancellation technique by circuit gain errors and PLL dynamics, respectively. Sections V and VI present methods for reducing the hardware complexity of the technique.

II. Overview of Phase-Noise Cancellation Technique

A high-level functional diagram of the integrated circuit (IC) presented in [1] is reproduced in Fig. 1. It includes all the components of a conventional second-order $\Delta\Sigma$ fractional-N PLL and some additional components which constitute the phase-noise cancellation technique. These additional components are indicated by the shaded blocks in the figure. The segmented mismatch shaping DAC encoder and the two banks of 1-b current DACs together constitute a DAC, which is, henceforth, referred to as the *cancellation DAC*. In the absence of the phase-noise cancellation technique, the quantization noise, $e_Q[n]$, from the second-order digital $\Delta\Sigma$ modulator effectively injects a charge sample, $Q_Q[n]$, into the loop-filter each reference period, thereby perturbing the voltage-controlled oscillator (VCO) and causing phase noise. The cancellation technique suppresses this phase noise by nominally injecting the charge sample $-Q_Q[n]$ into the loop-filter each reference period. Aside from a constant offset, the sequence of charge samples is well modeled as

$$Q_Q[n] = I_{CP}T_{\mathrm{VCO}} \sum_{k=n_0}^{n-1} e_Q[k] \tag{1}$$

where I_{CP} is the nominal charge-pump current, $T_{\rm VCO}$ is the nominal period of the PLL output, and $n_0 < n$ is an arbitrary starting time index. The phase-noise cancellation technique generates an estimate of $-Q_Q[n]$ by digitally computing $e_Q[n]$, reducing its bit-width using the third-order digital $\Delta\Sigma$ modulator, accumulating the result, and using the cancellation DAC to generate proportional analog charge samples. The cancellation DAC generates the charge samples by injecting appropriately scaled current pulses which are four VCO periods wide. The combination of the third-order digital $\Delta\Sigma$ modulator, the integrator, and the cancellation DAC is referred to as the *DAC cancellation path*. Note that while the pseudo-random bit generator is a part of some conventional $\Delta\Sigma$ fractional-N PLLs, it is shaded in the figure to emphasize its essential role in the phase-noise cancellation technique. Sections III, V, and VI describe the role in detail

The goal of the phase-noise cancellation technique is to remove all of $Q_Q[n]$ without introducing other sources of error. However, gain mismatches between the charge-pump and cancellation DAC cause a portion of $Q_Q[n]$ to be left behind in the loop-filter every reference period. Similarly, requantization of $e_Q[n]$ in the cancellation path, mismatches among the 1-b current DACs, and 1-b dithering contribute additional error charge along with that left behind by imperfect cancellation of $Q_Q[n]$. In spite of these imperfections, the system in Fig. 1 achieves a low phase noise[1] while maintaining a minimum bandwidth of 460 kHz. In order to achieve the same peak spot phase noise without the phase-noise cancellation technique, a PLL bandwidth of no more than 50 kHz would be required. This bandwidth extension is the principal benefit of the phase-noise cancellation technique. The success of the technique results from several architectural choices:

- use of a second-order digital $\Delta\Sigma$ modulator to choose the frequency division ratios;
- use of cancellation DAC current pulses with durations of 4-VCO periods;
- use of a third-order digital $\Delta\Sigma$ modulator with which to requeantize $e_Q[n]$ to 8-b;
- use of a segmented mismatch shaping DAC encoder;
- use of 1-b dither.

As is shown in the remainder of the paper, the first two choices determine the bandwidth and phase-noise performance limits of the cancellation technique. The other choices reduce the hardware complexity of the DAC cancellation path while ensuring that phase noise due to the requantization error, dither, and mismatches among the 1-b DACs is free of spurious tones and otherwise negligible.

The analysis offers design guidelines for how to customize the phase-noise cancellation technique to $\Delta\Sigma$ fractional-N PLLs of other specifications. For instance, one might use a second-order digital $\Delta\Sigma$ modulator to requantize $e_Q[n]$ instead of a third-order $\Delta\Sigma$ modulator, or requantize $e_Q[n]$ to 4-b instead of 8-b. The analysis is performed in the context of a system that uses the same general architecture as shown in Fig. 1 but possibly differs in the parameters of the PLL and the above mentioned choices. Expressions are derived that predict the power spectral density (PSD) of the PLL phase noise caused by errors in the DAC cancellation path. These expressions are explicit functions of most of the above mentioned choices. For example, one of the expressions is a function of the duration of DAC current pulses. A designer can use the expressions to pick values for the above choices that ensure that the PLL phase noise is small enough to meet specific requirements. To avoid burdening the designer with too many equations, qualitative recommendations are presented to serve as design guidelines in customizing the phase-noise cancellation technique.

For ease of reference, the digital $\Delta\Sigma$ modulator used to choose the sequence of division ratios is, henceforth, called a *fractional modulator*, and the digital $\Delta\Sigma$ modulator which requantizes $e_Q[n]$ is called the *requantization modulator*.

[1]For example, at 3 MHz from the PLL center frequency the phase noise is -127 dBc/Hz.

III. Fractional Modulator Order

Any mismatch between the charge-pump current and the cancellation DAC current causes phase noise in the PLL output. This phase noise tends to dominate the contributions of other errors in the cancellation path such as requantization and mismatches among the 1-b DACs. This section studies the impact of the order of the fractional modulator, L, on the phase noise caused by the mismatch. The requantization of $e_Q[n]$ is ignored to simplify analysis.

Suppose that $I_{\rm DAC}$ in amperes is the nominal gain of the cancellation DAC, and $x_{\rm DAC}[n]$ is its (unitless) input sequence. Then, the cancellation DAC generates current pulses which have nominal current values $i_{\rm DAC}^{[n]} = -1_{\rm DAC} x_{\rm DAC}^{[n]}$. Since the requantization of $e_Q[n]$ is ignored, it follows from Fig. 1 that $x_{\rm DAC}[n]$ is just the sum of all the past values of $e_Q[n]$

$$x_{\rm DAC}[n] = \sum_{k=n_0}^{n-1} e_Q[k].$$

Suppose that $T_{\rm DAC}$ is the nominal duration of the cancellation DAC current pulses. Therefore, the charge added to the loop-filter by the cancellation path is

$$Q_{\rm cancel}[n] = i_{\rm DAC}[n] \cdot T_{\rm DAC} = -I_{\rm DAC} T_{\rm DAC} \sum_{k=n_0}^{n-1} e_Q[k].$$

It follows from (1) that to cancel $Q_Q[n]$, $T_{\rm DAC}$, and $I_{\rm DAC}$ must satisfy $I_{\rm DAC} T_{\rm DAC} = I_{CP} T_{\rm VCO}$. Suppose that there is a normalized mismatch β between the charge-pump current and $I_{\rm DAC}$ i.e., the cancellation DAC has a gain of $(1+\beta) I_{\rm DAC}$ instead of $I_{\rm DAC}$. Then

$$Q_{\rm cancel}[n] = -(1+\beta) I_{CP} T_{\rm VCO} \sum_{k=n_0}^{n-1} e_Q[k]. \qquad (2)$$

Therefore, $Q_{\rm cancel}[n] \neq -Q_Q[n]$, and a portion of $Q_Q[n]$ remains in the loop-filter and causes phase noise. The order of the fractional modulator, L, determines the severity of this effect.

A. Phase-Noise Contribution

Fig. 2 presents a signal-processing model that predicts the phase noise as a function of β. Note that except for the shaded

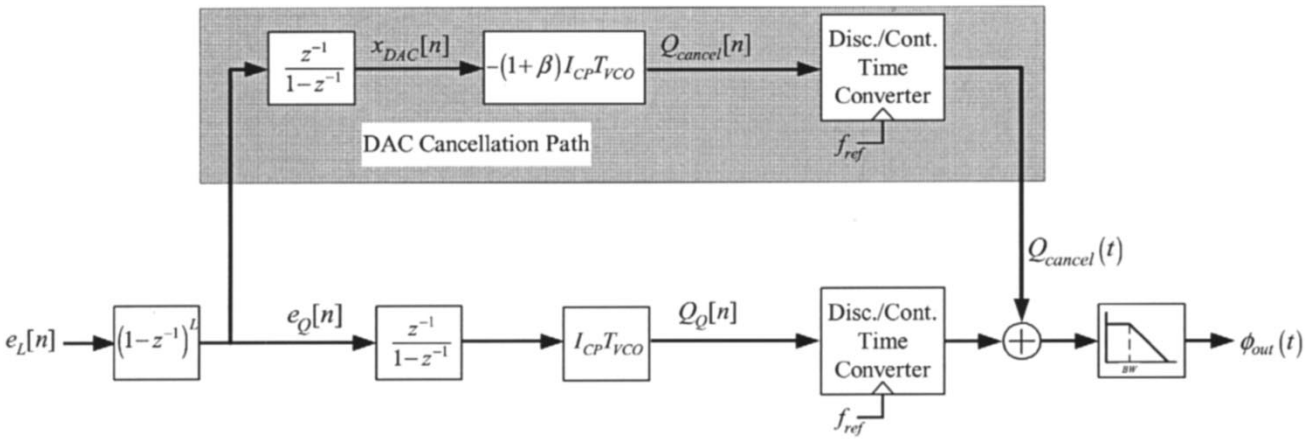

Fig. 2. Signal-processing model for technique including a gain error in the cancellation path.

portion, the model is well known [7], [8]. The shaded portion represents the DAC cancellation path when requantization of $e_Q[n]$ is ignored, as given by (2). The model output is the PLL phase noise. The low-pass filter in the model represents the response of the PLL to charge samples added to its loop-filter. It is expressed as $(2\pi/I_{CP}T_{\rm VCO})A_\phi(s)$ where $A_\phi(s)$ is the well-known, closed-loop transfer function from the reference to the output in a PLL, normalized to unity gain in the pass band [7], [9]. It is determined by the parameters of the PLL, and its -3-dB cutoff frequency is the bandwidth of the PLL. For instance, the PLL core in Fig. 1 results in

$$A_\phi(s) \approx \frac{1}{1+\frac{s}{K}+\frac{s^2}{\sqrt{b}K^2}}$$

where

$$K = \frac{I_{CP}RK_{\rm VCO}}{2\pi(N+a)}$$

$$b = 1+\frac{C_2}{C_1}.$$

The effect of adding a sequence of charge samples to the loop-filter is modeled by converting the sequence into a continuous-time signal and applying the result to the input of the low-pass filter. Since $Q_Q[n]$ and the cancellation charge samples, $Q^{[n]}_{\rm cancel}$ are both added to the loop-filter, they are converted into continuous-time charge signals, summed and applied to the input of the low-pass filter. Note that the conversion into continuous-time charge signals is at the rate of the reference frequency, $f_{\rm ref}$, because when the PLL is in lock, both $Q_Q[n]$ and $Q^{[n]}_{\rm cancel}$ are effectively added to the loop-filter at the rate of one sample each per every reference period. The relation between $Q_Q[n]$ and the quantization noise from the fractional modulator, $e_Q[n]$, which is given by (1), is explicitly shown in the model. The quantization noise, $e_Q[n]$, is modeled as an additive error source, $e_L[n]$, passing through L discrete differentiators.

As suggested in [10], in nonoverloading $\Delta\Sigma$ modulators of order $L \geqslant 2$, a 1-b dither signal added to the least significant bit (LSB) of the input ensures that $e_L[n]$ is white, and uniformly distributed over the range -0.5 to 0.5 with a variance of 1/12. The pseudo random bit generator shown in Fig. 1 provides this 1-b dither.[2] For $e_L[n]$ to have these properties, it is essential that the fractional modulator has enough output levels such that its internal quantizer never overloads. For instance, in [1], a fractional modulator of order $L = 2$ with a five-level quantizer is used to achieve an input no-overload range of -0.5 to 0.5.

The two-sided PSD[3] of the PLL phase noise due to the gain mismatch follows from the model:

$$S^{\beta}_{\phi}(j2\pi f) = \beta^2\frac{\pi^2}{3f_{\rm ref}}\left|2\sin\left(\frac{\pi f}{f_{\rm ref}}\right)\right|^{2(L-1)} \times |A_\phi(j2\pi f)|^2 \,{\rm rad}^2/{\rm Hz} \tag{3}$$

where $f_{\rm ref}$ is the reference frequency and f is the frequency offset relative to the PLL center frequency. Note that with $\beta = 1$, (3) reduces to the well-known expression for the PSD of the phase noise due to quantization noise in a conventional Lth-order $\Delta\Sigma$ fractional-N PLL [7], [8]. Equation (3) can be used to determine the value of L that satisfies the phase noise and bandwidth specifications for an expected β. For example, in the system in Fig. 1, $f_{\rm ref} = 48$ MHz, the normalized mismatch is expected to be at most 10% i.e., $\beta \leqslant 0.1$, and the required bandwidth is 460 kHz [1]. The target specifications require that the PLL phase noise is less than -120 dBc/Hz at a 3-MHz offset from the PLL center frequency. The poles and zeros of $A_\phi(s)$ were chosen to ensure that the PLL has a 67° phase margin. Consequently, $|A_\phi(j2\pi f)|$ is about -20 dB at $f = 3$ MHz. Substituting these values into (3) indicates that while $L = 2$ meets the phase-noise specification, $L = 1$ does not.

B. Recommended Fractional Modulator Order

Often, the above calculation has to be repeated for a number of offset frequencies, f, to choose an acceptable value for L.

[2]The 1-b dither also causes phase noise, which is usually negligible and is considered in a later section.

[3]The two-sided PSD value in dBrad per hertz is numerically equal to the single side-band phase noise in dBc per hertz units. Consequently, the various plots of the two-sided PSD of phase noise in this paper refer to dBc per hertz values.

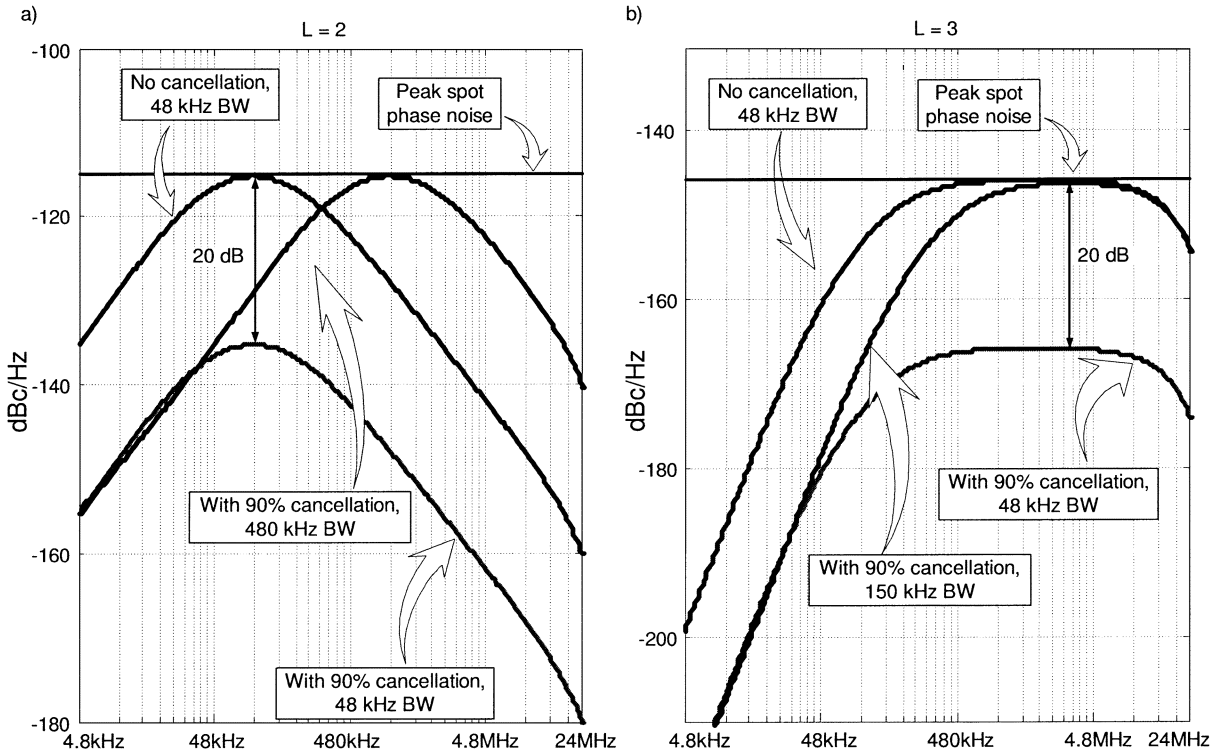

Fig. 3. Illustration of bandwidth extension made possible by the phase-noise cancellation technique.

Moreover, many of the PLL parameters which effect the above calculation (e.g., the poles and zeros of $A_\phi(s)$, and the reference frequency) are also choices available to the designer, necessitating many iterations of the above calculation to complete the design. Therefore, choosing a value for L is not always as straightforward as in the above example. This section simplifies the problem by showing that $L = 2$ or 3 are the best choices for many $\Delta\Sigma$ fractional-N PLLs.

It follows from (3), that the phase-noise cancellation technique reduces the spot phase noise caused by $e_Q[n]$ in a $\Delta\Sigma$ fractional-N PLL by $-20\log_{10}|\beta|$ decibels. The reduced phase noise can be traded off to increase the PLL bandwidth. Fig. 3 illustrates the tradeoff for the system depicted in Fig. 1. The PLL parameters are chosen such that $A_\phi(s)$ effectively has two poles—one at its passband edge and the other at roughly five times the bandwidth. The top and bottom curves in Fig. 3(a) are plots of $S_\phi^\beta(j2\pi f)$ where $A_\phi(s)$ has a 48-kHz bandwidth, $L = 2$, and $\beta = 1$ and 0.1, respectively. In other words, they respectively represent phase-noise PSDs in a second-order $\Delta\Sigma$ fractional-N PLL without the DAC cancellation path and with a 90% accurate DAC cancellation path. The 20-dB reduction implies that the $A_\phi(s)$ can now have a ten-fold wider bandwidth, namely 480 kHz, and still maintain the same peak spot phase noise, as indicated by the middle curve in the figure. A similar bandwidth extension is possible for a third-order $\Delta\Sigma$ fractional-N PLL, as illustrated by Fig. 3(b). However, note that the bandwidth extension in this case is only three-fold. Similarly, going to a higher order than $L = 3$ further reduces the bandwidth extension offered by the technique. Since a wide bandwidth is desirable for a variety of reasons, the achievable bandwidth extension is considered to be the principal benefit of the phase-noise cancellation technique [1]. Choices $L = 2$ or 3 offer the greatest bandwidth extension without complicating the requirements of other components of the PLL.

Suppose that without the cancellation technique, $A_\phi(s)$ has a bandwidth BW_{old} and achieves a certain peak spot phase noise. Suppose that the phase-noise reduction allows $A_\phi(s)$ to have a wider bandwidth BW_{new} while maintaining the same peak spot phase noise. The achievable bandwidth extension is then defined as $\lambda = BW_{\text{new}}/BW_{\text{old}}$. The achievable bandwidth extension is expected to depend on L, and the locations of the poles and zeros of $A_\phi(s)$. However, as shown in Appendix A, an approximate but reasonable estimate for the achievable bandwidth extension is

$$\lambda \approx \left|\frac{1}{\beta}\right|^{\frac{1}{(L-1)}} \tag{4}$$

which is independent of $A_\phi(s)$. For instance, for $\beta = 0.1$, ten-fold, three-fold, and two-fold bandwidth extension is possible for $\Delta\Sigma$ fractional-N PLLs with $L = 2, 3,$ and 4, respectively. This is illustrated by the plots shown in Fig. 3. It follows from (4) that only a small bandwidth extension is achieved for orders $L > 3$.

Fractional modulators of order $L > 3$ are undesirable for other reasons as well. It can be shown [11] that they need more output levels than lower- order modulators to ensure that $e_L[n]$, and, hence, the PLL phase noise have no spurious tones. This complicates the design of the frequency divider because more output levels imply a wider range of frequency division ratios. The resulting charge-pump current pulses are also wider and contribute more charge-pump noise. Another problem arises because charge-pump current pulses do not occur uniformly in

time—the start of a charge-pump pulse sometimes coincides with a rising edge transition of the reference signal, while at other times it coincides with the rising edge transition of the divider output signal. This time-variant behavior has the effect of applying a nonlinearity to the quantization noise, $e_Q[n]$. Consequently, high-frequency components of $e_Q[n]$ fold to lower frequencies and increase close-in phase noise. The effect is aggravated for $L > 3$ because the spectrum of $e_Q[n]$ is such that it has more power in the higher frequencies.

Fractional modulators of order $L = 1$ are not recommended either since they cause a lot of phase noise close to the PLL center frequency. This is evident from the absence of any zeros at dc in the expression for $S_\phi^\beta(j2\pi f)$ in (3) when $L = 1$. The reason is that when $L = 1$, the phase noise caused by $e_Q[n]$, even after cancellation, does not have the familiar high-pass spectral shape. The example calculation in Section III-A, which picked $L = 2$ over $L = 1$, illustrates this claim.

IV. DAC Current Pulse Duration

The duration of the DAC current pulse, $T_{\rm DAC}$, affects the PLL phase noise in two ways. First, any static error in the DAC current pulse duration causes incomplete removal of $Q_Q[n]$, just like the gain mismatch, β, considered in Section III. Second, the nonzero width of the DAC current pulses allows $Q_Q[n]$ to disturb the VCO before being removed by the DAC current pulses. This phenomenon is described in detail later. First, the error in $T_{\rm DAC}$ is considered. Requantization error is ignored in the following discussion.

A. Gain Errors Due to Imperfect Pulse Timing

Suppose that the $\Delta\Sigma$ fractional-N PLL changes from one center frequency to a new center frequency such that the nominal period of the VCO changes from $T_{\rm VCO}$ to $T_{\rm VCO}^*$. In this case, the charge effectively added to the loop-filter by $e_Q[n]$ is

$$Q_Q[n] = I_{CP}T_{\rm VCO}^* \sum_{k=n_0}^{n-1} e_Q[k].$$

As described previously, to remove $Q_Q[n]$ it is necessary to ensure that $I_{CP}T_{\rm VCO}^* = I_{\rm DAC}T_{\rm DAC}$. If $T_{\rm DAC}$ does not change with $T_{\rm VCO}$, this does not happen. Consequently, a portion of $Q_Q[n]$ is left in the loop-filter, similar to the effect of a normalized gain mismatch, β. The recommended solution is to make $T_{\rm DAC}$ equal an integer number of VCO periods, i.e., $T_{\rm DAC} = M_{\rm DAC}T_{\rm VCO}$ where $M_{\rm DAC}$ is an integer. Then, as $T_{\rm VCO}$ varies so does $T_{\rm DAC}$ and $I_{CP}T_{\rm VCO}^* = I_{\rm DAC}T_{\rm DAC}$ is satisfied. The frequency divider, which operates by counting an integer number of VCO periods, can be easily modified to generate a pulse whose duration is equal to a specified integer number of VCO periods.

Even so, inevitable timing errors in the circuitry that generates the cancellation DAC current pulse cause its duration to be $(T_{\rm DAC} + \Delta T_{\rm DAC})$ resulting in a normalized gain error of $\Delta T_{\rm DAC}/T_{\rm DAC}$ in the cancellation path. The PLL phase noise contributed by this gain error can be predicted by adding $\Delta T_{\rm DAC}/T_{\rm DAC}$ to β in (3)

$$\beta_{\rm eff} = \beta + \frac{\Delta T_{\rm DAC}}{T_{\rm DAC}}.$$

Usually, these timing errors do not scale with $T_{\rm DAC}$. For example, suppose the circuitry that generates the cancellation pulse has a timing error of at least 20 ps,[4] and that the DAC current pulse is four VCO periods wide. At 2.4 GHz, this results in a normalized gain error of 1.2%. A simple way to ensure that these timing errors do not limit the PLL phase noise is to choose a wide cancellation DAC current pulse to ensure that $\Delta T_{\rm DAC}/T_{\rm DAC} \ll \beta$, but as described below this causes other problems.

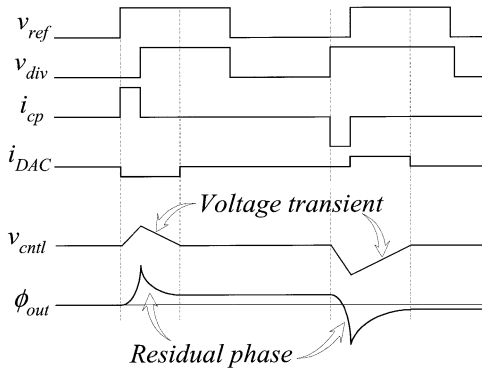

Fig. 4. Mechanism of imperfect phase-noise cancellation.

B. Nonzero DAC Current Pulse Width

Wide cancellation pulses are not very effective in canceling the phase-noise contributions of narrow charge-pump pulses. Even if they remove $Q_Q[n]$ completely, they disturb the VCO in doing so and cause phase noise. This phenomenon is illustrated in Fig. 4, where, for the sake of simplicity, dither and modulation signals are ignored, it is assumed that the loop-filter comprises just one capacitor i.e., $R = C_1 = 0$ in Fig. 1, and the PLL is assumed to be in frequency and phase lock. The waveforms labeled i_{CP} and $i_{\rm DAC}$ in Fig. 4 represent the current pulses that are added to the loop-filter by the charge-pump and the cancellation path, respectively. The waveforms labeled $v_{\rm cntl}$ and $\phi_{\rm out}$, respectively, represent the input voltage of the VCO and the PLL phase noise, $\phi_{\rm out}(t)$. Assuming that the cancellation path has no gain error, the charge added by $i_{\rm DAC}$, i.e., $Q_{\rm cancel}[n]$, exactly cancels out that added by i_{CP}, i.e., $Q_Q[n]$, as illustrated by $v_{\rm cntl}$ returning to its original value at the end of each cancellation DAC pulse. However, the ramp-like voltage transients in $v_{\rm cntl}$ disturb the VCO. These disturbances are accumulated into a residual phase, as shown in the figure.

If the charge-pump and the cancellation DAC pulses were of the same width, or better, if they were both impulses, the phase-noise cancellation would have been complete. While the very narrow charge-pump pulses can be modeled as impulses, the same is not true for the wide-cancellation DAC pulses. As the figure suggests, the wider the cancellation DAC pulses, the larger the voltage transients and the residual phase. The effect

[4]This is not a pessimistic estimate considering that a typical inverter delay in 1.8-V, 0.18-μm CMOS technology is about 60 ps.

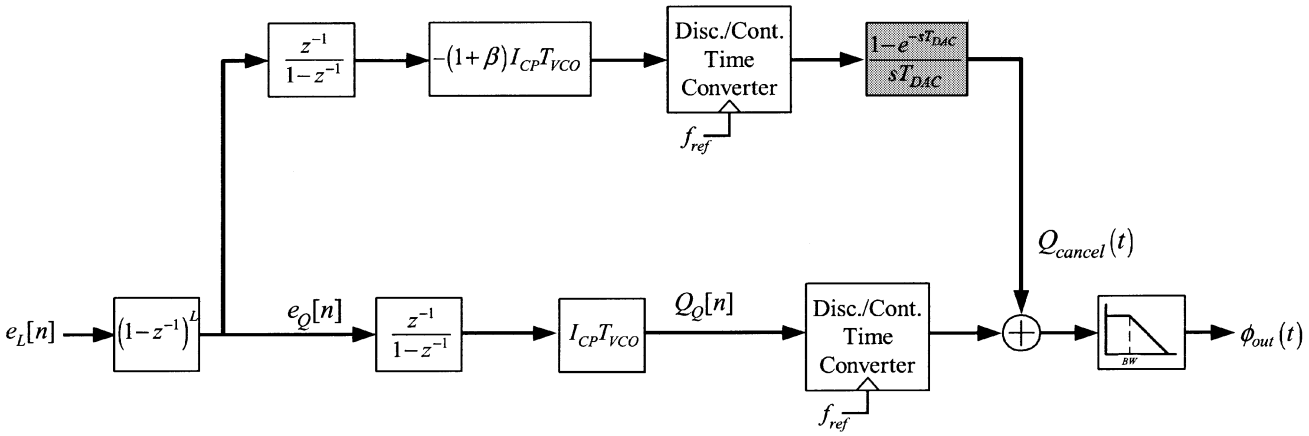

Fig. 5. Extension of the phase-noise cancellation model to include effects of cancellation pulsewidths.

of the nonzero width of the cancellation DAC pulses can be incorporated into the model by adding a zero-order hold block in the cancellation path, as indicated by the shaded block in Fig. 5. Appendix B justifies this modification and clarifies the inherent assumptions. Using the approximation[5] $e^{-x} = 1 - x + x^2/2$, the zero-order hold block can be reduced to a left plane zero, $(1+sT_{\rm DAC}/2)$. Consequently, an expression for the PSD of the residual PLL phase noise can be obtained from the model

$$S_\phi^{\beta,T_{\rm DAC}}(j2\pi f) \approx \left\{\beta^2 + (\pi f T_{\rm DAC})^2\right\} \frac{\pi^2}{3f_{\rm ref}} \times \left|2\sin\left(\frac{\pi f}{f_{\rm ref}}\right)\right|^{2(L-1)} |A_\phi(j2\pi f)|^2 \ \text{rad}^2/\text{Hz} \qquad (5)$$

where it is assumed that $|\beta| \ll 1$. The effect of nonzero $T_{\rm DAC}$ is represented by the $\pi f T_{\rm DAC}$ term in the expression.

The validity of (5) is demonstrated in Fig. 6 in which plots of $S_\phi^{\beta,T_{\rm DAC}}(j2\pi f)$ are compared to simulated phase-noise PSDs. The simulations correspond to a second-order $\Delta\Sigma$ fractional-N PLL with a 480-kHz bandwidth and an ideal cancellation path (i.e., a DAC cancellation path without requantization or component errors). The smooth curves are plots of $S_\phi^{\beta,T_{\rm DAC}}(j2\pi f)$ for $T_{\rm DAC} = 4$, 8, 16, and 32 VCO periods, and the ragged curves are simulated phase-noise PSDs for the same set of values of $T_{\rm DAC}$. For comparison, simulated and theoretical plots of phase-noise PSDs for the same PLL, but without the cancellation path, are included. Note that (5) does not accurately predict the simulated PSDs at frequency offsets less than 1 MHz, because it does not include the phase-noise contributed by the 1-b dither added to the input of the fractional modulator in Fig. 1. Section VI addresses the dither contribution in more detail.

The small fractional spur visible in the simulated curves is not predicted by (5). It is caused by the nonuniform occurrence of the charge-pump pulses. The start of a charge-pump pulse varies from one reference period to another; while sometimes it coincides with the rising edge transition of the reference waveform, at other times it coincides with the rising-edge transition of the divider-output waveform. This time-variant behavior is responsible for the spurious tone. The spurious tone occurs in the conventional $\Delta\Sigma$ fractional-N PLL as well, but is masked by the phase noise caused by $e_Q[n]$. When the phase-noise cancellation technique removes most of $e_Q[n]$, this spurious tone is uncovered. The spurious tone is, however, so small that it is often dominated by spurious tones caused by other nonlinearities in the PLL.

[5]The approximation is good for frequencies, $f \ll 2/T_{\rm DAC}$. For instance, in the system in Fig. 1, in which $T_{\rm DAC} = 4T_{\rm VCO}$, the approximation is good for frequencies, $f \ll f_{\rm VCO}/2$.

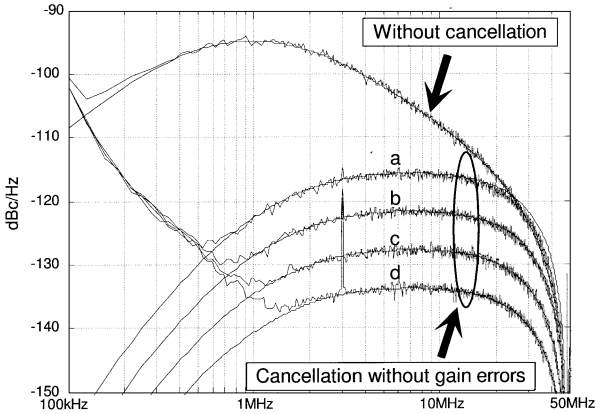

Fig. 6. Solid lines and ragged curves, respectively, represent predicted and simulated phase-noise PSD for the cancellation technique for DAC pulses of duration *(a)* 32, *(b)* 16, *(c)* 8, and *(d)* 4-VCO periods.

Equation (5) can be used to choose a $T_{\rm DAC}$ which satisfies the phase noise and bandwidth specifications for an expected normalized gain mismatch, β. Alternatively, $T_{\rm DAC}$ may be chosen such that $\pi f_{\rm crit} T_{\rm DAC} \ll \beta$, where $f_{\rm crit}$ is the critical frequency offset at which it is most difficult to meet the phase-noise requirements of a particular $\Delta\Sigma$ fractional-N PLL. For instance, for the system in [1] $f_{\rm crit} = 3$ MHz and the expected gain mismatch is at most 10% i.e., $\beta = 0.1$. Therefore, the constraint implies that $T_{\rm DAC} \ll 10$ ns or about 26 VCO periods. The choice used in the system is $T_{\rm DAC} = 4$ VCO periods. The corresponding phase noise is indicated by the bottom most curve in Fig. 6 which is about 14-dB below the phase-noise requirement of -120 dBc/Hz of the system.

C. Recommended Cancellation DAC Current Pulse Duration

Before recommending a choice for $T_{\rm DAC}$, it is useful to enumerate the inferences of Section IV-A and -B:

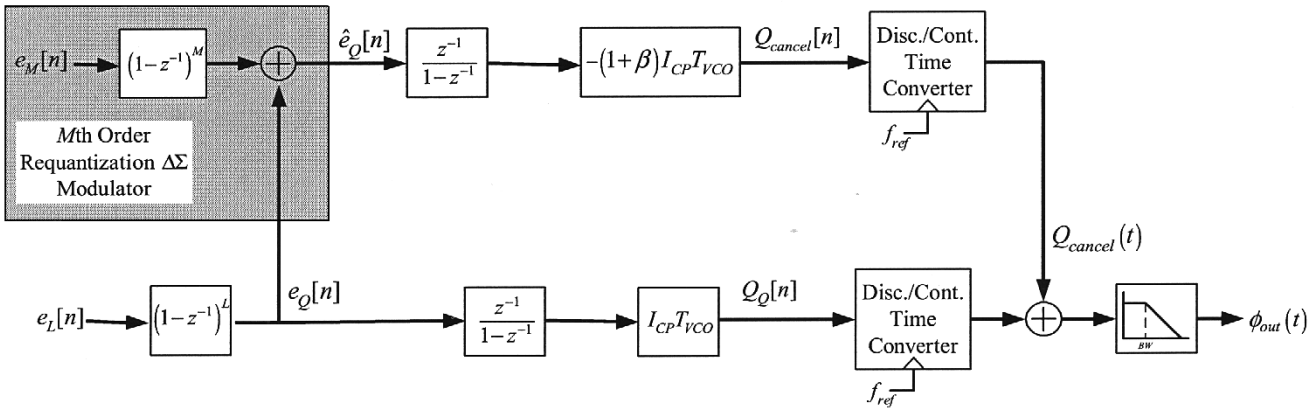

Fig. 7. Signal-processing model of the cancellation technique that includes the requantization $\Delta\Sigma$ modulator.

- $T_{\rm DAC}$ must be an integer number of VCO periods, $T_{\rm DAC} = M_{\rm DAC}{}^{*}T_{\rm VCO}$,
- $T_{\rm DAC}$ must be large enough so that $\Delta T_{\rm DAC}/T_{\rm DAC} < \beta$,
- $T_{\rm DAC}$ must be small enough that $\pi f_{\rm crit} T_{\rm DAC} \ll \beta$.

The recommended duration is $T_{\rm DAC} = M_{\rm DAC}{}^{*}T_{\rm VCO}$, where $M_{\rm DAC}$ is an integer chosen as a compromise between the last two constraints. For instance, suppose that the expected normalized mismatch is 10%, i.e., $\beta = 0.1$, the timing error is $\Delta T_{\rm DAC}$ =40 ps, the nominal VCO period, $T_{\rm VCO}$, is approximately 400 ps, and the critical frequency offset is $f_{\rm crit}$ =3 MHz. Then the last two constraints, respectively, require that $M_{\rm DAC} \gg 1$ and $M_{\rm DAC} \ll 26$. In [1], a good compromise was found to be $M_{\rm DAC} = 4$.

V. Requantization

The purpose of requantizing $e_Q[n]$ is to reduce the required performance of the cancellation DAC. For instance, in Fig. 1, if $e_Q[n]$ were not requantized, the cancellation DAC would have to be a 15-b DAC. Moreover, its LSB would correspond to a current on the order of a few nanoamperes. Requantization allows the use of only a 7-b DAC with an LSB corresponding to 10-μA. The penalty is an increase in the PLL phase noise.

Suppose that a zero sample delay,[6] unity gain, Mth-order digital $\Delta\Sigma$ modulator requantizes $e_Q[n]$ and that the requantized sequence, $\hat{e}_Q[n]$, has a LSB of Δ_{RQ}. For instance, in Fig. 1, $\hat{e}_Q[n]$ is an 8-b number taking on values in the range -2 to 2 corresponding to an LSB of 1/64. The requantization error, $\hat{e}_Q[n] - e_Q[n]$, causes an error charge to be added to the loop-filter every reference period. The amount of the phase-noise contributed by requantization is determined by M and Δ_{RQ}. The relationship is derived below ignoring the effects of nonzero cancellation pulse widths to simplify the analysis.

A. Phase-Noise Contribution

The effect of requantization on the PLL phase noise is incorporated into the model in Fig. 2 by adding a requantization error term as indicated by the shaded portion in Fig. 7. The requantization error is modeled as an additive source, $e_M[n]$, passing through M discrete differentiators. Using analyzes similar to those presented in [10], it can be shown that 1-b dither added to the input of the fractional modulator ensures that $e_M[n]$ is white, uncorrelated with $e_L[n]$ and its delayed versions, is uniformly distributed from $-0.5\Delta_{RQ}$ to $0.5\Delta_{RQ}$, and has a variance of $\Delta_{RQ}^2/12$. For this to be true, it is essential for the Mth-order $\Delta\Sigma$ modulator to have enough output levels such that its internal quantizer never overloads. An expression for the PSD of the phase-noise contributed by the requantization error follows from the model:

$$S_{\phi}^{RQ}(j2\pi f) \approx \frac{\Delta_{RQ}^2 \pi^2}{3 f_{\rm ref}} \left| 2\sin\left(\frac{\pi f}{f_{\rm ref}}\right)\right|^{2(M-1)} |A_{\phi}(j2\pi f)|^2 \tag{6}$$

where it has been assumed that β is much less than unity. Equation (6) can be used to determine values of M and Δ_{RQ} which satisfy the phase noise and bandwidth specifications.

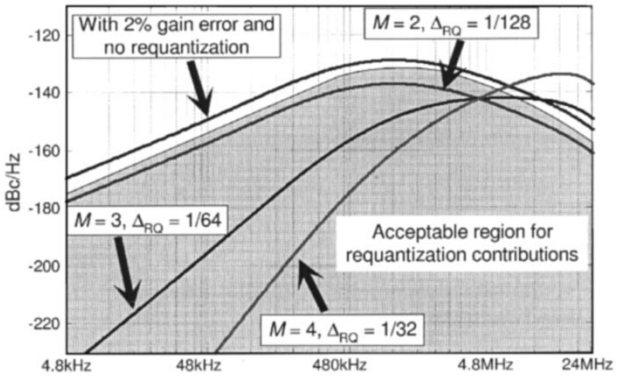

Fig. 8. Illustration of the effects of requantization on the phase noise of the PLL output.

B. Recommended M and Δ_{RQ}

The recommended choices are $M = L$ or $L+1$, where L is the order of the fractional modulator, and the requantization LSB satisfy $\Delta_{RQ} < \beta$. As shown below, these choices ensure that the phase noise caused by requantization error is negligible compared to that caused by DAC cancellation path gain mismatch. This in turn ensures that requantization does not limit the phase-noise performance of the $\Delta\Sigma$ fractional-N PLL.

In the absence of requantization, nonzero cancellation pulse width effects, and other DAC errors, the lowest phase noise which the cancellation technique can guarantee is $S_{\phi}^{\beta}(j2\pi f)$

[6]If the requantization digital $\Delta\Sigma$ modulator were to have a few samples of delay, the delay could be accounted for by appropriately delaying the fractional modulator output sequence $y[n]$ in Fig. 1.

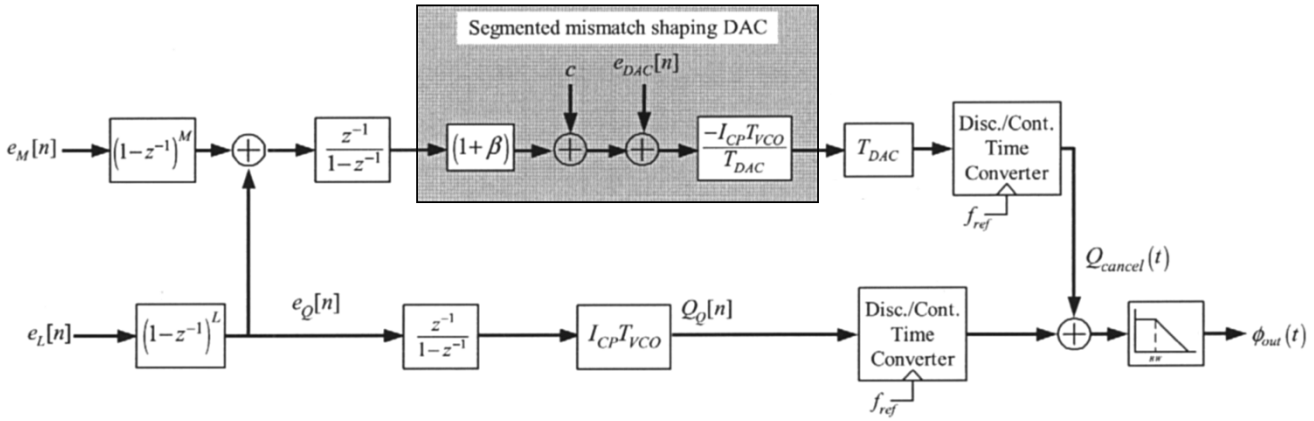

Fig. 9. Signal-processing model of the cancellation technique including the segmentation of the DAC.

given in (3). Therefore, choosing M and Δ_{RQ} such that $S_\phi^{RQ}(j2\pi f) < S_\phi^{\beta}(j2\pi f)$, ensures that requantization error does not limit phase-noise performance. In this respect, it is useful to compare the two quantities

$$\frac{S_\phi^{RQ}(j2\pi f)}{S_\phi^{\beta}(j2\pi f)} \approx \frac{\Delta_{RQ}^2}{\beta^2}\left|2\sin\left(\frac{\pi f}{f_{\text{ref}}}\right)\right|^{2(M-L)}. \qquad (7)$$

One choice that ensures that the $S_\phi^{RQ}(j2\pi f) < S_\phi^{\beta}(j2\pi f)$ is $M = L$ and $\Delta_{RQ} < \beta$. However, by using $M > L$, it might be possible to requantize more coarsely so as to further reduce the required performance of the cancellation DAC.

The possibility is illustrated in Fig. 8, which corresponds to a 480-kHz bandwidth, second-order $\Delta\Sigma$ fractional-N PLL with the phase-noise cancellation technique. The top curve is the expected PLL phase noise due to a 2% gain error and no requantization in the cancellation path. Requantization will not noticeably increase the PLL phase noise if $S_\phi^{RQ}(j2\pi f)$ is restricted to the shaded region, which starts about 3-dB below the top curve. Plots of $S_\phi^{RQ}(j2\pi f)$ for orders $M = L$, $L+1$ and $L+2$ (i.e., $M = 2$, 3 and 4), and for specific values of Δ_{RQ} are included. In each case, the largest Δ_{RQ} was chosen that ensures that $S_\phi^{RQ}(j2\pi f)$ lies mostly within the shaded region. The choices $M > L$ allow coarser quantization, but for high frequencies, the requantization contributions are larger than those due to the gain error alone. At least for $M = L+1$, this is not particularly worrisome since $S_\phi^{RQ}(j2\pi f)$ is still much less than the peak spot phase noise.

VI. Miscellaneous Factors

A. Segmented Mismatch Shaping DAC Encoder

The combined output of the two DAC banks can be modeled using an offset, a gain error, and a normalized additive error source, $e_{\text{DAC}}[n]$, as shown by the shaded blocks in Fig. 9. The DAC error, $e_{\text{DAC}}[n]$, is caused by mismatches among the 1-b DAC elements. It causes phase noise. The constant offset has no noticeable effect on the PLL phase noise, the gain error has already been considered in Section III.

The segmented mismatch shaping encoder controls the operation of the DAC banks such that $e_{\text{DAC}}[n]$ is uncorrelated with the input to the DAC, spurious-free, and has a zero at dc. It follows from the model that the contribution of $e_{\text{DAC}}[n]$ to the PLL phase-noise PSD is

$$S_\phi^{\text{DAC}}(j2\pi f) = \frac{1}{f_{\text{ref}}} S_{\text{DAC}}(e^{j2\pi f T_{\text{ref}}}) \cdot |A_\phi(j2\pi f)|^2 \qquad (8)$$

where $S_{\text{DAC}}(e^{jw})$ is the PSD of $e_{\text{DAC}}[n]$. The zero at dc ensures that $S_{\text{DAC}}(e^{jw})$ and hence $S_\phi^{\text{DAC}}(j2\pi f)$ has very little power in frequencies close to the PLL center frequency.

The segmented mismatch shaping encoder exploits redundancy in the DAC banks to guarantee that $e_{\text{DAC}}[n]$ has the aforementioned properties. While multiple methods of realizing the encoder have been reported [12]–[15], none of them offer closed form expressions for $S_{\text{DAC}}(e^{jw})$. Therefore, simulations are relied upon to determine the degree of mismatch among the DAC elements that can be tolerated. As reported in [16], it may be possible to derive closed form expressions for $S_{\text{DAC}}(e^{jw})$ if detailed statistics of the quantization noise are available. Another alternative is to use reported bounds on the power in low-frequency bands [17] to make some approximate quantitative predictions about tolerable mismatches.

B. Number of Input Bits in the Fractional Modulator

The digital hardware complexity of the cancellation path can be reduced by allocating only a few bits to the input of the fractional modulator. The reason is that both the fractional and requantization modulator have data paths which are at least as wide as the input of the fractional modulator. However, a lower limit is imposed on the number of input bits by 1-b dither employed by the cancellation technique.

Suppose that K bits are allocated to the input of the fractional modulator. Therefore, 1-b dither added to the LSB of the input of the fractional modulator contributes undesirable FM modulation of $\pm f_{\text{ref}}/2^K$. The models presented so far have neglected the effect of dither in comparison with other sources of error. However, if K is small, the undesired FM modulation could degrade the signal-to-noise ratio of the transmitted frequency modulation signal. Even in the absence of frequency modulation, it causes f^{-2} noise in the PLL output phase which could be significant at low-frequency offsets as shown by the simulated PSDs in Fig. 6. While these effects are well understood by prior art, they are usually dominated by the other sources of noise in the $\Delta\Sigma$ fractional-N PLL.

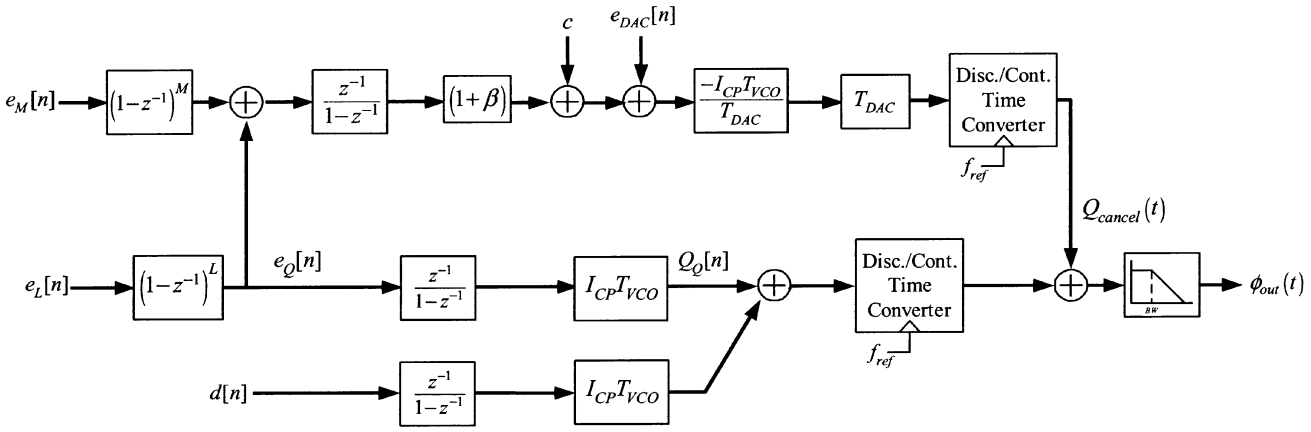

Fig. 10. Signal-processing model of the cancellation technique including dither.

Note that the 1-b dither can not be altogether eliminated since its absence would cause strong fractional spurs in the PLL phase. It is however tempting to modify $Q_{\text{cancel}}[n]$ to cancel contributions from dither as well. This promises to allow the use of as few bits K as possible. The possibility becomes evident by considering Fig. 10, which includes 1-b dither in the signal processing model. The dither can be added to $e_Q[n]$ before requantization by the Mth order $\Delta\Sigma$ modulator. Rather surprisingly, including the dither in the cancellation path causes spurious tones to reappear in the PLL phase noise. It negates the claims made in Sections III-A and V about the spurious-free nature of $e_M[n]$ and $e_{\text{DAC}}[n]$. Simulations corroborate this counter-intuitive phenomenon and it can be proved following analyses similar to those in [10]. However, the proof is not included in this paper.

VII. Conclusion

A theoretical analysis of the phase-noise cancellation technique applied to a $\Delta\Sigma$ fractional-N PLL has been presented. The influence of circuit errors on the effectiveness of the phase-noise cancellation technique has been analyzed and quantified. A fundamental lower limit on the phase noise imposed by the use of a current DAC for the phase-noise cancellation has been derived. Recommendations have been made that enable customization of the phase-noise cancellation technique in response to specific PLL target specifications.

Appendix A

The achievable bandwidth extension depends on L and the location of the poles and zeros of $A_\phi(s)$. Suppose that in a conventional Lth order $\Delta\Sigma$ fractional-N PLL, $A_\phi(s) = A_{\text{old}}(s)$ where $A_{\text{old}}(s)$ is a low-pass filter of bandwidth BW_{old}. It can be approximately[7] represented as

$$A_{\text{old}}(s) = \prod_{k=1}^{R} \frac{1}{1+\frac{s}{2\pi f_k}}$$

where f_k is the kth pole frequency, R is the number of poles, and $f_1 = BW_{\text{old}}$. It is assumed for now that $A_{\text{old}}(s)$ has no complex poles. Suppose that when the phase-noise cancellation technique is applied, then $A_\phi(s) = A_{\text{new}}(s)$ where $A_{\text{new}}(s)$ is a low-pass filter of bandwidth BW_{new}. Define the achievable bandwidth extension as $\lambda \triangleq BW_{\text{new}}/BW_{\text{old}}$. It is also assumed that the poles of $A_{\text{new}}(s)$ are all scaled by λ. This is a reasonable assumption since it would impart the same phase margin to the core PLL. Therefore, it can be represented as

$$A_{\text{new}}(s) = \prod_{k=1}^{R} \frac{1}{1+\frac{s}{2\pi\lambda f_k}}.$$

Now the phase-noise contributed by $e_Q[n]$ without cancellation technique is

$$S_\phi^{\text{old}}(j2\pi f) = \frac{\pi^2}{3f_{\text{ref}}}\left|2\sin\left(\frac{\pi f}{f_{\text{ref}}}\right)\right|^{2(L-1)}|A_{\text{old}}(j2\pi f)|^2.$$

It has two parts—$A_{\text{old}}(j2\pi f)$ and unfiltered phase noise, which increases at the rate of $20^*(L-1)$ dB/decade until $0.5^* f_{\text{ref}}$. To prevent the spot phase noise for $f < 0.5^* f_{\text{ref}}$ from becoming too large, the Lth order $\Delta\Sigma$ fractional-N PLL has at least $(L-1)$ poles in $A_{\text{old}}(s)$. Then, $S_\phi^{\text{old}}(j2\pi f)$ reaches its maximum value when $f = f_{L-1}$, or in other words, it peaks when $(L-1)$ poles of $A_{\text{old}}(s)$ "kick in." Assuming that $f_{L-2} \neq f_{L-1}$, $|A_{\text{old}}(j2\pi f)|$ can be approximated as

$$|A_{\text{old}}(j2\pi f)| \approx \prod_{k=1}^{L-1}\frac{f_k}{f} \quad \forall f \gg f_{L-1}.$$

Using the above approximation and using $\sin(x) \approx x$ for small x i.e., for $f \ll f_{\text{ref}}$, it follows that the peak spot phase noise is approximately

$$\max\left\{S_\phi^{\text{old}}(j2\pi f)\right\} \approx \frac{\pi^2}{3f_{\text{ref}}}\left(\frac{2\pi}{f_{\text{ref}}}\right)^{2(L-1)}\prod_{k=1}^{L-1} f_k^2.$$

Proceeding similarly, it can be shown that the peak spot phase noise for the system with the phase-noise cancellation technique is approximately

$$\max\left\{S_\phi^{\text{new}}(j2\pi f)\right\} \approx \beta^2\frac{\pi^2}{3f_{\text{ref}}}\left(\frac{2\pi}{f_{\text{ref}}}\right)^{2(L-1)}\prod_{k=1}^{L-1}(\lambda f_k)^2.$$

The achievable bandwidth extension is obtained by equating the above two peak spot phase-noise values. Equating them results

[7]Type-II PLLs have an in-band pole-zero doublet, which is ignored in this argument.

in $1 \approx \beta^2\lambda^{2(L-1)}$ from which it follows that the achievable bandwidth extension is $\lambda \approx |1/\beta|^{1/(L-1)}$. Note that the argument can be extended to include complex poles in $A_\phi(s)$ provided that the $(L-1)$th pole is itself not a complex pole.

APPENDIX B

In the system in Fig. 1, once every reference period, the phase-noise cancellation technique generates a pulse of current $i_{\rm DAC}[n]$, which has a duration of $T_{\rm DAC}$ seconds, starting from the rising edge transition of the divider output waveform. The resulting waveform can be denoted as

$$Q_{\rm cancel}(t) = \sum_{n=0}^{\infty} i_{\rm DAC}[n]\{u(t - t_{\rm div}[n]) - u(t - t_{\rm div}[n] - T_{\rm DAC})\}$$

where $u(t)$ is the unit-step function, the PLL is assumed to start at $n = 0$, and $t_{\rm div}[n]$ is the time when the frequency divider finishes its division cycle and produces a rising edge transition. The rising edge transitions of the divider output waveform are not uniformly spaced in time. However, for the purposes of this model, they can be approximated as $t_{\rm div}[n] \simeq nT_{\rm ref}$ and the above equation can be modified to

$$\begin{aligned} Q_{\rm cancel}(t) &= p(t) * \hat{Q}_{\rm cancel}(t) \\ \text{where } p(t) &= \frac{1}{T_{\rm DAC}}\{u(t) - u(t - T_{\rm DAC})\} \\ \text{and } \hat{Q}_{\rm cancel}(t) &= \sum_{n=0}^{\infty} i_{\rm DAC}[n] \cdot T_{\rm DAC} \cdot \delta(t - nT_{\rm ref}). \end{aligned}$$

Note that the approximation holds true even in the presence of small static-phase offsets inevitably caused by charge-pump current mismatches. The impulse train $\hat{Q}_{\rm cancel}(t)$ is the same as the output of the discrete-time to continuous-time converter acting on $Q_{\rm cancel}[n]$ in Fig. 5. Its convolution with $p(t)$ is represented by a multiplication in the Laplace domain by the Laplace transform of $p(t)$

$$\frac{1 - e^{-sT_{\rm DAC}}}{sT_{\rm DAC}}.$$

This is the transfer function of the well-known zeroth-order hold block.

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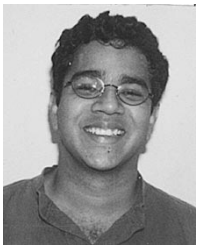

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