Techniques for In-band Phase Noise Suppression in Re-circulating DLLs

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Abstract

This paper presents a re-circulating delay-locked loop (DLL) with various innovations to improve in-band phase noise suppression. The voltage-controlled oscillator (VCO) and bias circuitry incorporate circuit-level techniques that reduce 1/f noise through switched biasing. The phase realignment theory presented in [1] is applied to optimize the VCO so as to maximize the phase noise suppression achieved by periodically switching in a clean reference pulse, and it is further applied to optimize the loop filter. Theoretical predictions are verified through a 100 MHz prototype IC fabricated in a 0.18 μm CMOS process.

Introduction

Frequency synthesizers are critical blocks in communication systems. Ring oscillator VCOs are widely used in low-performance frequency synthesizer applications such as clock multiplication for digital systems because of their simplicity, wide tuning range, and ease of integration. However, they are less commonly used in communication applications wherein low phase noise is required, because they tend to introduce excessive close-in phase noise. In a conventional phase-locked loop (PLL) frequency synthesizer, the loop bandwidth is usually constrained to less than 5% of the reference frequency to maintain stability across process and temperature extremes, so the PLL only provides limited attenuation of the VCO phase noise.

To overcome this barrier, a clean reference pulse can be injected periodically into the VCO so as to reset the phase error and thereby suppress the noise memory caused by the jitter accumulation effect in the VCO. The result is significant attenuation of the in-band phase noise. This noise reduction technique, referred to as *phase realignment* in the remainder of the paper, can be implemented in various ways. In a DLL based clock multiplier the delay of a voltage-controlled delay Line (VCDL) is locked to the reference period [2]. Multiple delayed versions of the reference clock from the VCDL are then combined to produce the final clock signal. Since the delayed reference is discarded at the end of the VCDL, phase realignment is performed naturally, by design. Another type of DLL, referred to as a *re-circulating DLL* in the remainder of the paper, is implemented using a ring VCO with the phase realignment performed by periodically opening the ring to discard the noisy VCO edge and replace it with a clean reference edge [3]. Alternatively, in a *realigned PLL* [1], the phase realignment is performed by directly coupling a strongly buffered version of a clean reference source into one of the inverters in the VCO. The strong buffer overpowers the VCO inverter so that the VCO phase is "dragged" toward the correct position.

As demonstrated in [1], in both the re-circulating DLL and the realigned PLL, parasitic coupling among the delay cells in the VCO tends to degrade the phase realignment and leads to incomplete noise memory suppression. Therefore the choice of VCO topology is critical in effectively implementing the phase realignment technique.

On the device level, $1/f$ noise tends to severely degrade the in-band phase noise performance of the VCO. In analogy to the phase realignment technique, $1/f$ noise can be suppressed by periodically switching the associated transistors on and off so as to suppress the long term noise correlation [4] [5].

This paper presents a re-circulating DLL with a novel ring VCO topology. The VCO is optimized for the phase realignment technique and also exploits switched biasing to suppress $1/f$ noise. The phase realignment theory from [1] is applied to provide design guidelines and optimize the loop parameters. The fabricated IC can be configured as a conventional PLL and a re-circulating DLL. Measurement results are presented that closely support the theoretical findings.

Theoretical Model

A theoretical model is presented in [1] that characterizes the phase noise performance of both DLLs and realigned PLLs. It is based on physical observations that the phase of the VCO is shifted almost instantaneously when the phase realignment occurs and that the phase shift is nearly linear with respect to the instantaneous phase difference between the VCO and the reference. The ratio between the phase shift and the phase difference just before realignment is defined as β and referred to as the *realigning factor*. The value of β ranges from 0 to 1 and is a measure of how completely the phase error is suppressed. The attenuation of VCO phase noise increases as β increases. Therefore a large β is desirable when a noisy VCO is used.

Conventional frequency analysis on the DLL mainly focuses on the stability and settling of the loop [6],[7]. On the other hand, quantitative analysis of conventional DLLs is usually done in the time domain [8], [9], because DLLs are used mainly in digital applications where jitter performance is of interest. Although jitter is a popular figure of merit, it is difficult to separate the contribution to the jitter from individual noise sources in the circuit using the published analyses. To optimize the loop filter parameters in a re-circulating DLL, the theory in [1] is applied here without modification except that both first and second-order loop filters are considered.

As demonstrated below, the results indicate that when the VCO noise is dominant and a clean reference source is used, a second-order filter offers no benefit over a first-order filter, and increasing the loop filter bandwidth actually improves the attenuation of in-band VCO phase noise. Moreover,

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while the choice of loop filter bandwidth significantly affects the attenuation of the VCO phase noise and input noise, i.e., the charge pump and divider noise, it has little affect on the attenuation of the reference noise. Thus, although a small bandwidth can result in less jitter based on the conventional analysis [9], it does not necessarily lead to low in-band phase noise, especially when the noise is dominated by the VCO. These general observations are quantified below for the re-circulating DLL prototype.

Switched Biasing For 1/f Noise Reduction

The concentration of $1/f$ noise power at low frequencies indicates there is a long-term self-correlation. A widely accepted theory for the source of $1/f$ noise in MOS transistors is the trapping and releasing of carriers in the gate oxide. As shown in [4] and [5], interruption of the noise correlation by periodically switching the MOSFET between "on" and "off" states results in a significant reduction in 1/f noise. When the transistor is turned off, the trapped carriers tend to be released, resulting in the reset of the noise source. This phenomenon is analogous to the phase realignment technique wherein the phase error is reset so as to suppress the phase noise memory.

Circuit Details

Fig. 1 shows the simplified block diagram of the proposed synthesizer. The VCO contains two NAND gates and several voltage controlled delay cells [10]. When the signals "rlgn" and "pulse_sw" are set high, the NAND gates act as inverters and the VCO behaves as a conventional ring VCO. Phase realignment is performed in two steps. First by setting "rlgn" and "pulse_sw" low, the noisy VCO edge is blocked and the "ring" is temporarily opened. Then, when the clean reference edge arrives it causes both "rlgn" and "pulse_sw" to go high so as to start a new cycle of oscillation free of phase noise memory. The implementation of the phase realignment technique is functionally equivalent to that presented in [3].

To minimize the $1/f$ noise, switched biasing is used in both the voltage controlled delay cell and its biasing circuitry. Because the loop filter is single-ended, the bias circuitry must generate the control voltages for both the PMOS and NMOS transistors in the delay cell to ensure symmetry of the waveform, which is critical for $1/f$ noise reduction [11]. Fig. 2(a) shows a simple implementation of the bias. Despite its simplicity, the $1/f$ noise generated from this bias can significantly degrade the VCO phase noise. Conventional approaches for $1/f$ noise reduction are to increase the size of the device or to filter the control voltage. Neither approach is area-efficient and filtering potentially affects the loop dynamics.

A straightforward switched biasing approach is shown in Fig 2(b). It consists of two identical bias branches that are used alternately with only one on at any time. As shown in Fig. 2(c), the branch not in use is switched off by setting the gate-source voltage to 0. While the approach has the desired effect of suppressing $1/f$ noise, the switching introduces the equivalent of a parasitic resistor between the loop filter node and the power supply, which can adversely affect the loop dynamics.

To alleviate this problem, the bias circuit shown in Fig 3(a) is used in the re-circulating DLL prototype. This circuit switches the source and drain to turn off each transistor as illustrated in Fig. 3(b). For example, when an NMOS transistor is turned off, its source and drain are both switched to V_{DD}. Thus, the gate-source voltage is negative in the "off" state, and the threshold voltage is increased by the increased source-bulk voltage, which also helps to release the trapped carriers. The clock for the switched biasing is provided by the VCO itself. To demonstrate the effect of the switched biasing during testing, the devices are sized such that the VCO in-band phase noise is dominated by the bias noise and the switched biasing can be disabled for comparison.

The performance of the voltage controlled delay cells in the VCO are critical. Their phase noise and value of β strongly depend their circuit topology. As described in [1], to maximize β it is necessary to minimize the coupling among delay cells and ensure that each cell is truly edge-triggered. The proposed delay cell is an extension of that shown in Fig. 4(a), wherein the delay is varied by controlling the transconductance of M_p, M_n, M_p' and M_n'. This topology minimizes the inter-cell coupling because, except for the delay control lines, the delay cells are only connected through low impedance power supply lines. Transistor level simulations confirm that the resulting VCO achieves a β of very nearly 1, the theoretical maximum, across process corners. The topology also allows rail-to-rail signal swing and a wide tuning range (1 MHz to 160 MHz) to cover the large component spread in typical CMOS processes.

The pseudo-differential topology is used to reject common mode noise from the supply and substrate. Normally, the differential signal is created using a latch with two back-to-back inverters at the outputs as shown in Fig. 4(a). In a normal oscillating cycle, every transistor is turned fully on and off. However if the conventional latch is used, when M_p, M_n, M_p' and M_n' are off, unlike the other transistors their gate-source voltages are not set to zero. In order to exploit the switched biasing technique to further suppress $1/f$ noise in these transistors, a special latch is implemented as shown in Fig. 4(b). Using M_n as an example, when it is turned off using the proposed latch, both its source and drain are pulled to V_{DD}. The "off" state is identical to the "off" state of the transistor in the bias described above.

Measurement Results

The die photo is shown in Fig. 9 and the system specifications are summarized in Table I. As described below, Figures 5-8 present measured results with superimposed theoretical results in close agreement.

Fig. 5 shows superimposed measured and theoretically calculated phase noise power spectral density (PSD) curves for the synthesizer configured as conventional PLL and as a re-circulating DLL with a 2nd order loop filter, both with and without switched biasing. The system parameters are also shown in the figure. The results indicate that phase realignment significantly attenuates the in-band VCO phase noise. With the switched biasing is enabled, a peak spot phase noise reduction of 5 dB is observed in both the PLL and the re-circulating DLL. Since the transistor in the delay cell is switched off the same fashion as in the bias, it is reasonable

to expect similar noise attenuation is achieved inside the delay cell. This result confirms that the switched biasing technique is feasible up to at least 100 MHz. With both noise reduction schemes enabled, a peak spot phase noise reduction of 21.5 dB is observed compared to the conventional PLL. Fig. 6 shows the measured phase noise when the synthesizer is configured as a re-circulating DLL with a 1st-order loop filter. The results support the assertions made above based on the theory presented in [1] that a wide-band 1st-order loop filter yields the best results.

In the theoretical calculations, the VCO stand-alone phase noise is required. This was obtained by measuring the phase noise of the system with and without switched biasing and with a very narrow bandwidth so that the phase noise is dominated by the VCO. Because the in-band phase noise was dominated by the VCO, it was difficult to measure the input and reference noise transfer functions from the phase noise. In order to characterize the two transfer functions, a sinusoid was ac coupled into the loop filter and the reference clock pin, respectively. This injected signal, which is shaped by the noise transfer function, is upconverted to the synthesizer output in the form of spurious tones around the VCO center frequency. The power of the spurs were then measured using a spectrum analyzer. Sweeping the frequency of the injected signal provided a sampled version of the noise transfer function.

Due to the parasitic capacitance and inductance from the PCB board, it was difficult to measure the absolute value of the transfer functions. Alternatively, since the input noise transfer function of a conventional PLL is well known, it was used as a reference and the measured results for the re-circulating DLL with 2nd and 1st order loop filters were normalized with respect to the conventional PLL. Fig. 7 shows the input phase noise transfer functions of the conventional PLL, and re-circulating DLL with 2nd and 1st loop filters. As shown in the figure, for the same total loop filter capacitance, the DLL with a 1st order loop filter provides more attenuation to input noise than that with a 2nd order loop filter. Fig. 8 shows the reference noise transfer function of the conventional PLL, re-circulating DLL with 22 μF loop filter and DLL with 2.2 nF loop filter. As expected, the loop filter bandwidth does not significantly affect the attenuation of reference noise.

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TABLE I
Performance and Specification Summary

Technology	1.8V, 0.18 μm CMOS (1 poly, 6 metal)
Chip Size	2.2mm x 2.2 mm
Package	32 Pin QFN
Reference Frequency	4MHz (derived from a 32 MHz crystal)
VCO Frequency	100MHz
Tuning Range	1MHz ~ 160MHz
Power Consumption	8.6mW (core)

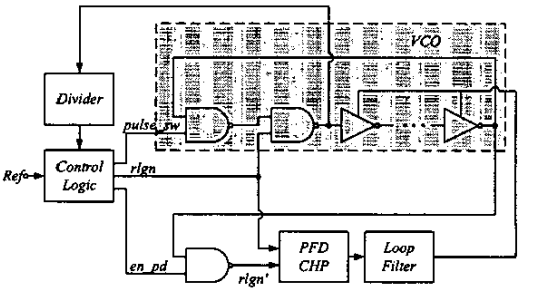

Figure 1: Simplified block diagram of the proposed synthesizer.

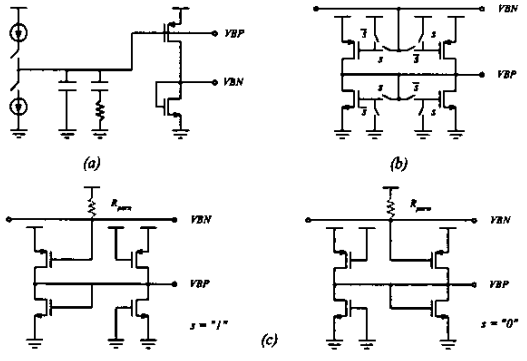

Figure 2: VCO bias (a) Simplest implementation. (b) One straightforward realization of the switched biasing. (c) Operation details.

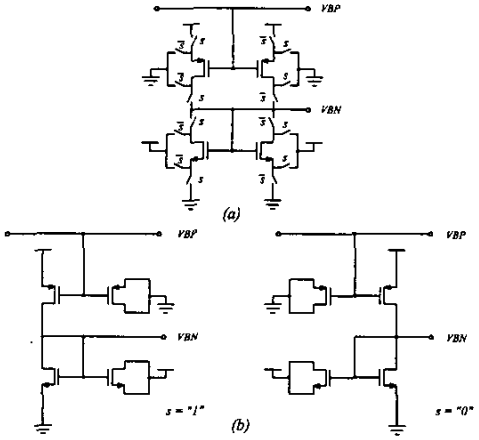

Figure 3: (a) Proposed bias generation. (b) Operation details.

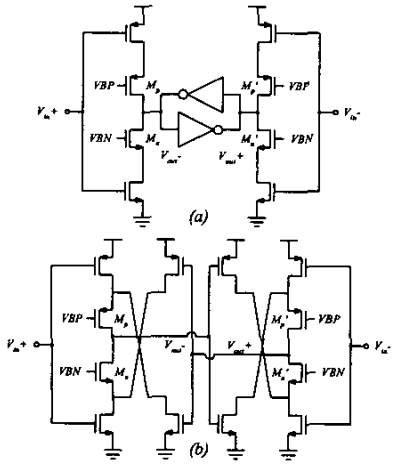

Figure 4: (a) Delay cell with conventional latch. (b) Proposed delay cell with improved β and a special latch for 1/f noise attenuation.

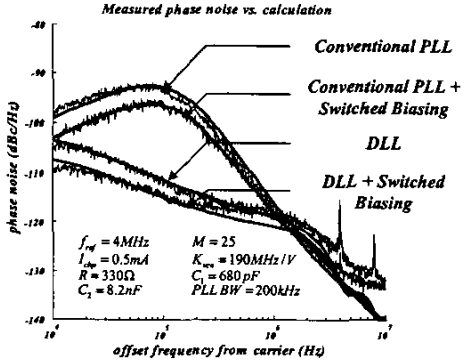

Figure 5: Measured phase noise of conventional PLL and re-circulating DLL with a 2nd order loop filter.

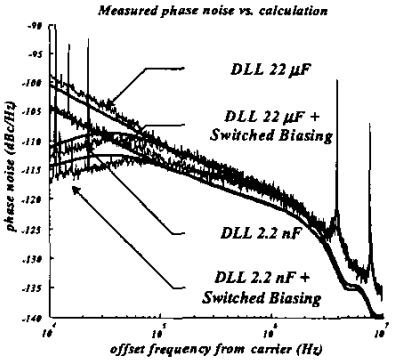

Figure 6: Measured DLL phase noise showing the effect of loop filter: wide loop bandwidth results in more VCO noise attenuation.

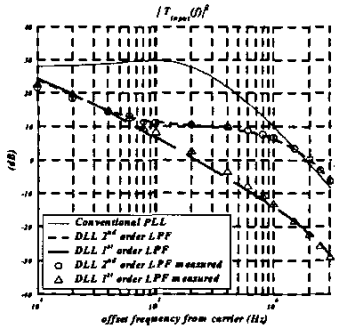

Figure 7: Measured input noise transfer function in PLL, re-circulating DLL with 2nd and 1st order loop filter.

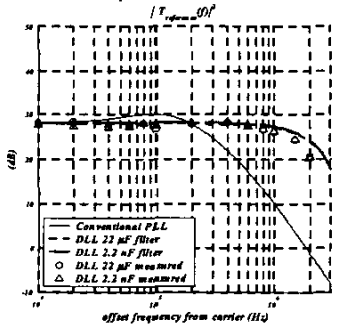

Figure 8: Measured reference noise transfer function in a DLL.

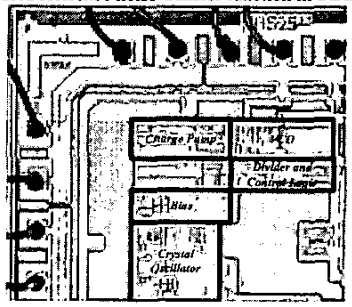

Figure 9: Die photograph