A Multiple-Crystal Interface PLL With VCO Realignment to Reduce Phase Noise

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***Abstract*—An enhancement to a conventional integer-N phase-locked loop (PLL) is introduced, analyzed, and demonstrated experimentally to significantly reduce voltage-controlled oscillator (VCO) phase noise. The enhancement, which involves periodically injection locking the VCO to a buffered version of the reference, has the effect of widening the PLL bandwidth and reducing the overall phase noise. It is demonstrated in a 3-V 6.8-mW CMOS reference PLL with a ring VCO capable of converting most of the popular crystal reference frequencies to a 96-MHz RF PLL reference and baseband clock for a direct conversion Bluetooth wireless LAN. The peak in-band phase noise at an offset of 20 kHz is −102 dBc/Hz with the technique enabled and −92 dBc/Hz with the technique disabled. A theoretical analysis is presented and shown to be in close agreement with the measured results.**

***Index Terms*—Delay-locked loop (DLL), phase-locked loops (PLLs), phase noise, voltage-controlled oscillators (VCOs).**

I. Introduction

THIS paper presents a new enhancement to a conventional PLL in which a CMOS ring voltage-controlled oscillator (VCO) is periodically realigned by the phase-locked loop (PLL) reference signal to reduce phase noise. The enhancement is applied to a VHF reference PLL capable of operation with a wide range of crystal frequencies for a Bluetooth transceiver. A peak phase noise reduction of 10 dB and an integrated phase noise reduction of 8.3 dB relative to the conventional PLL alone are demonstrated via measured results that closely match theoretical predictions.

The eventual market penetration of low-end LANs such as Bluetooth will depend largely on the extent to which transceiver prices can be reduced. With Bluetooth unit prices approaching the five-dollar level, the cost of the external crystal has become significant. Since the transceivers generally are placed in host devices with their own crystal references, such as cellular telephones, computers, and personal digital assistants, a cost reduction can be achieved by sharing the same reference as the host device. This is particularly advantageous in wireless host devices such as cellular telephones which tend to be sensitive to interference at the circuit board level from oscillator signals outside of their frequency plans. Therefore, for maximum flexibility, it is desirable to have a Bluetooth transceiver capable of operating from all of the popular crystal reference frequencies.

The most critical local oscillator in a wireless transceiver typically is that used to drive the RF mixers. In a direct conversion Bluetooth transceiver such as the one in [1], in-phase and quadrature local oscillator signals are required with frequencies selectable from 2.402 to 2.480 GHz in steps of 1 MHz. In principle, these signals can be generated from any of the popular crystal frequencies by a fractional-N RF PLL, but the flexibility required to accommodate all the crystal frequencies would translate into significant added circuit area and power consumption [2], [3]. Alternatively, an integer-N RF PLL with a 1-MHz reference signal can be used. The primary difficulty with this approach is that a reference PLL capable of generating the 1-MHz reference signal with very little phase noise from any of the crystal frequencies is required. This paper presents such a PLL designed for a next generation version of the Bluetooth transceiver in [1]. The PLL generates a 96-MHz signal from which the 1-MHz RF PLL reference is derived along with a 32-MHz clock used to drive the baseband circuitry and data converters in the transceiver.

The reference PLL design was challenging because of the requirements that it be implemented with only CMOS transistors, that it use an on-chip ring VCO to avoid external components, and that its phase noise between 1 and 50 kHz from the carrier be below −100 dBc/Hz (the loop bandwidth of the RF PLL is 50 kHz). Unfortunately, CMOS ring oscillators are noisy. For example, the measured phase noise from the ring VCO implemented within the reference PLL at an offset from the carrier of 100 kHz is −107 dBc/Hz, so the loop bandwidth of a conventional PLL would have to be approximately 100 kHz to sufficiently suppress the VCO noise with enough margin to allow for the phase noise contributed by the other PLL components. The large loop bandwidth ruled out the use of a conventional integer-N PLL. In such a PLL, the reference frequency is obtained by dividing the crystal frequency to its greatest common divisor with 96 MHz, but to maintain stability over process and temperature extremes the PLL reference frequency must be approximately 20 times the loop bandwidth [4]. Among the commonly used crystal references, this implies that the target phase noise could not be met for 19.68- and 19.8-MHz crystals using a conventional integer-N PLL. For example, the greatest common divisor of 19.68 and 96 MHz is 480 kHz, which implies a reference frequency of 480 kHz and a maximum practical loop bandwidth of only 24 kHz.

To solve this problem, a VCO realignment technique has been developed and applied to a conventional narrow band integer-N PLL. The new topology is referred to as a realigned

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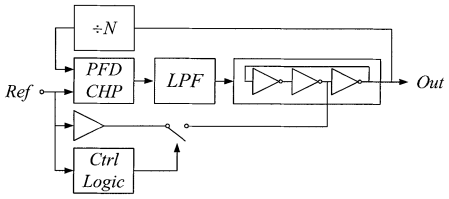

Fig. 1. Top-level system block diagram of the RPLL.

PLL (RPLL). The idea is to perform VCO realignment by injection locking the VCO to a buffered version of the PLL reference once every reference period. As explained in Section II, the realignment has the effect of significantly reducing the phase noise introduced by the VCO at frequencies below the reference frequency. A theoretical model of the RPLL is derived in Section III, and measurement results are presented in Section IV that are very close to those predicted by the theoretical model. It is shown that the RPLL has similarities to a delay-locked loop (DLL) in the way it suppresses phase noise below the reference frequency, and that the theoretical model derived in this paper for the RPLL is also applicable to the DLL. Nevertheless, along with the usual benefits offered by PLLs, the RPLL offers the potential advantage that it is not restricted to oscillators based on delay lines; the injection locking principle on which the RPLL is based is known to be applicable to various types of VCOs [5], [6].

II. Realigned PLL System Overview

A. The Idea

A simplified block diagram of the RPLL is shown in Fig. 1. The idea is to use a buffered version of the PLL reference to correct the VCO once every reference period. As shown in the figure, the new PLL is based on a conventional integer-N PLL with the addition of a buffer and a control logic block. The motivation for this new topology is described below.

If the oscillator were noiseless, its zero crossings would be uniformly spaced in time. However, noise inside the oscillator causes phase fluctuations which give rise to errors in the zero-crossing times. As shown in [7], noise-induced phase fluctuations persist indefinitely in oscillators. This phenomenon is illustrated in Fig. 2(a), where the phase fluctuations "build up" in a three-stage ring VCO over time because the zero-crossing error introduced by each inverter adds to all the previous zero-crossing errors [8]. Therefore, the VCO can be modeled as a phase fluctuation integrator. In the frequency domain, this integration has the effect of multiplying the power spectral density (PSD) of the zero-crossing time errors by a transfer function proportional to $1/f^2$ which results in high in-band phase noise.

As shown in Fig. 2(b), assuming that the VCO frequency is an integer multiple of the reference frequency, the realignment technique shorts a buffered version of the clean reference signal to the VCO output during windows surrounding the time instants where VCO edges ideally coincide with reference signal edges. This causes each VCO edge to be "pulled" toward the correct position, thereby suppressing the memory of past errors.

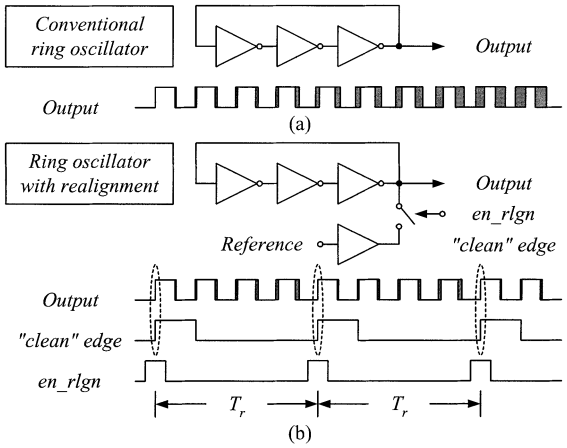

Fig. 2. (a) Phase noise is accumulated in typical ring oscillators. (b) Periodically realigning the oscillator to a "clean" edge suppresses the phase noise accumulation.

In the frequency domain, the suppression of noise memory attenuates the $1/f^2$ transfer function mentioned above at frequencies below the reference frequency which greatly reduces the in-band phase noise power introduced by the VCO.

B. The Realigning Factor

During each phase realignment, the buffered reference edge is connected to the VCO clock edge. Ideally, if both the reference and the VCO were noiseless, a VCO edge would line up with an edge of the buffered reference once every reference period. However, phase noise in the VCO and the reference cause these two edges to occur at slightly different times. The coupling between the VCO delay cell and the reference buffer causes the VCO edge to be dragged toward the reference edge. Inevitably, the realignment perturbs the VCO. As shown in [7], perturbations to the VCO generally cause both amplitude and phase fluctuations. The amplitude fluctuations usually disappear within several VCO cycles due to the amplitude limiting mechanism in oscillators. The phase fluctuations, however, persist indefinitely.

Transistor level simulation can be used to quantify the VCO's response to the phase realignment by examining the VCO phase shift several cycles after the phase realignment. Simulations indicate that the VCO phase is shifted almost instantaneously by the realignment. A typical plot of the phase shift as a function of the phase error, i.e., the difference between VCO and reference phases just prior to the realignment, is shown in Fig. 3. In practice, the cycle-to-cycle variation of the instantaneous phase error is mainly caused by the VCO phase noise, whose magnitude is usually small enough that the phase shift can be approximated as linear with respect to the phase error, as indicated by the "zoomed-in" plot in Fig. 3. The magnitude of the slope of the curve is defined as the realigning factor, and is denoted as β. The value of β ranges from 0 to 1 and describes the strength of the realignment. As depicted in Fig. 4, after the realignment the VCO phase is shifted by $-\beta\theta_e$ where θ_e is defined as the instantaneous phase error between the VCO and the reference just prior to the realignment.

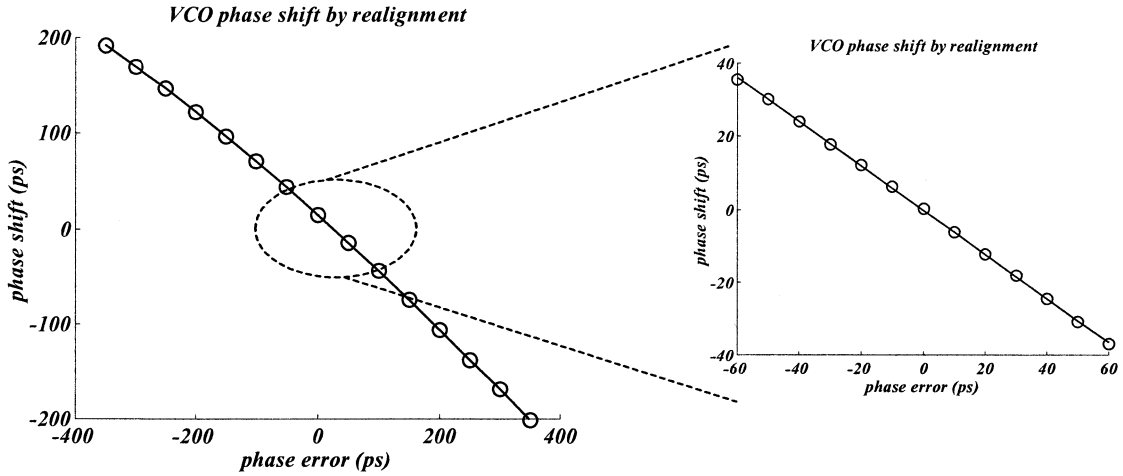

Fig. 3. Simulated shifted phase versus initial phase difference curve.

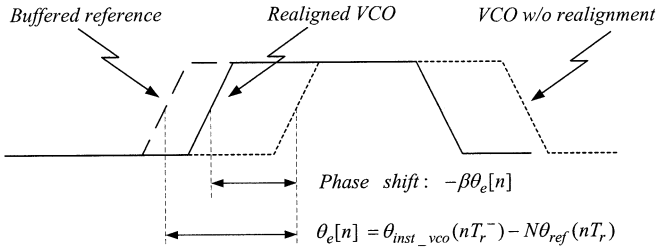

Fig. 4. Time-domain waveform of the realignment: the VCO phase shifts almost instantly and linearly to $\theta_e[n]$.

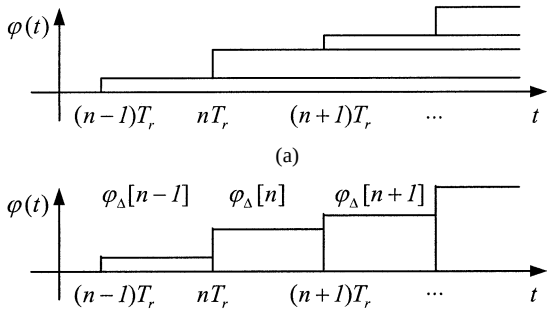

Fig. 5. The "extra" phase shift due to the phase realignment (a) shown as the sum of a series of phase steps and (b) shown as the result of passing an impulse train through a hold operation.

III. Theoretical Analysis

A. Phase Noise of the Realigned VCO

For the following analysis, it is assumed that the realignment shifts the VCO phase instantaneously and the phase shift is linear with respect to the instantaneous phase error by a factor of β. As mentioned above, these assumptions are supported by circuit simulations, and, as shown in Section V, they are also closely supported by measurement results. It is further assumed that the VCO frequency is N times the reference frequency, which is the case in a locked integer-N PLL. Thus, except for any systematic offset caused by path mismatches in the phase-frequency detector and charge pump, the instantaneous phase difference between nominally coincident VCO and the reference edges arises completely from circuit noise.

In the following, the reference phase error is denoted as $\theta_{\rm ref}(t)$, the VCO phase error that would have occurred in the absence of phase realignment is denoted as $\theta_{\rm vco}(t)$, and the "extra" phase shift caused by the phase realignment is denoted as $\varphi(t)$. Consequently, the instantaneous VCO phase error is given by

$$\theta_{\rm inst\_vco}(t) = \theta_{\rm vco}(t) + \varphi(t). \tag{1}$$

The phase realignment is performed at the reference edges, so the VCO phase is shifted at discrete times. As indicated in Fig. 4, the instantaneous phase difference between the VCO and the reference just before the nth realignment can be represented as a sequence given by

$$\theta_e[n] = \theta_{\rm inst\_vco}(nT_r^-) - N\theta_{\rm ref}(nT_r) \tag{2}$$

where T_r is the reference period and $t = nT_r^-$ denotes the time instant just before the nth reference edge. The factor N arises because the VCO frequency is N times the reference frequency and all the phase terms have the units of radians. After the nth phase realignment, the VCO is phase shifted by $-\beta\theta_e[n]$ based on the assumption that the phase shift is linear with respect to the phase error.

As mentioned above, the VCO can be modeled as a phase error integrator. Therefore, each phase realignment can be modeled as the addition of a step increment to the VCO phase; therefore, as depicted in Fig. 5(a), $\varphi(t)$ can be written as

$$\varphi(t) = -\beta \sum_{n=-\infty}^{\infty} \theta_e[n] \cdot u(t - nT_r). \tag{3}$$

Alternatively, as indicated in Fig. 5(b), $\varphi(t)$ can be viewed as the result of an impulse train $\sum_{n=-\infty}^{\infty} \varphi_\Delta[n] \cdot \delta(t - nT_r)$, passed through a "hold" operation, where

$$\varphi_\Delta[n] - \varphi_\Delta[n-1] \equiv -\beta\theta_e[n]. \tag{4}$$

Combining (3) and (4) gives

$$\varphi(t) = \sum_{n=-\infty}^{\infty} \varphi_{\Delta}[n] \cdot h_{\text{hold}}(t - nT_r) \tag{5}$$

where $h_{\text{hold}}(t) = u(t) - u(t - T_r)$ is the impulse response of the hold operation. Thus, (5) represents a discrete-to-continuous-time (D/C) conversion obtained by holding the value of $\varphi(t)$ equal to $\varphi_{\Delta}[n]$ throughout the time interval $nT_r \leq t < (n+1)T_r$. Taking the Fourier transform of (5) yields

$$\varphi(j\omega) = T_r e^{-j\omega T_r/2} \cdot \frac{\sin(\omega T_r/2)}{\omega T_r/2} \cdot \varphi_{\Delta}(z)\Big|_{z=e^{j\omega T_r}} \tag{6}$$

where $\varphi_{\Delta}(z)$ is the z transform of $\varphi_{\Delta}[n]$.

To make use of this result, an expression for $\varphi_{\Delta}(z)$ is required. Combining (2) and (4) gives

$$\varphi_{\Delta}[n] - \varphi_{\Delta}[n-1] = -\beta(\theta_{\text{vco}}[n] + \varphi_{\Delta}[n-1] - N\theta_{ref}[n]). \tag{7}$$

Taking the z transform of (7) and solving for the z transform of $\varphi_{\Delta}[n]$ results in

$$\varphi_{\Delta}(z) = \frac{-\beta}{1 + (\beta - 1)z^{-1}}\,\theta_{\text{vco}}(z) + \frac{N\beta}{1 + (\beta - 1)z^{-1}}\,\theta_{\text{ref}}(z). \tag{8}$$

Combining (1), (6), and (8) results in[1]

$$\theta_{\text{inst\_vco}}(j\omega) = \theta_{\text{vco}}(j\omega)H_{rl}(j\omega) + \theta_{\text{ref}}(j\omega)H_{up}(j\omega) \tag{9}$$

where

$$H_{rl}(j\omega) = 1 - \frac{\beta}{1 + (\beta - 1)e^{-j\omega T_r}}\, e^{-j\omega T_r/2} \frac{\sin(\omega T_r/2)}{\omega T_r/2} \tag{10}$$

and

$$H_{\text{up}}(j\omega) = \frac{N\beta}{1 + (\beta - 1)e^{-j\omega T_r}}\, e^{-j\omega T_r/2} \frac{\sin(\omega T_r/2)}{\omega T_r/2}. \tag{11}$$

The transfer function $H_{rl}(j\omega)$ represents the effect of the phase realignment and the transfer function $H_{\text{up}}(j\omega)$ represents the up-conversion of the reference noise to the VCO output.

B. Linearized Phase Noise Model for the RPLL

Without the realignment technique, the PLL phase noise $\theta_{\text{out}}(s)$ is described by the well-known linearized model in the s domain as shown in Fig. 6(a), where K_{chp} and K_{vco} are the charge pump and VCO gains, respectively, and $H_{\text{lp}}(s)$ is the transfer function of the PLL loop filter [4]. The reference phase noise $\theta_{\text{ref}}(s)$, divider phase noise $\theta_{\text{div}}(s)$, and the charge pump phase noise $\theta_{\text{chp}}(s)$ are all considered to be *input noise* and the PLL applies the same transfer function to each of them.

The results derived above can be applied to this model to obtain a model of the RPLL without violating any of the assumptions underlying the original PLL model. Specifically,

[1]The sampling of $\theta_{\text{vco}}(t)$ and $\theta_{\text{ref}}(t)$ inevitably causes aliasing as both signals are not band-limited. However, the aliasing effect is neglected when converting the discrete time results to continuous time because the loop bandwidth of the PLL is small compared with the reference frequency. This approximation is consistent with the assumptions underlying the conventional PLL analysis [4].

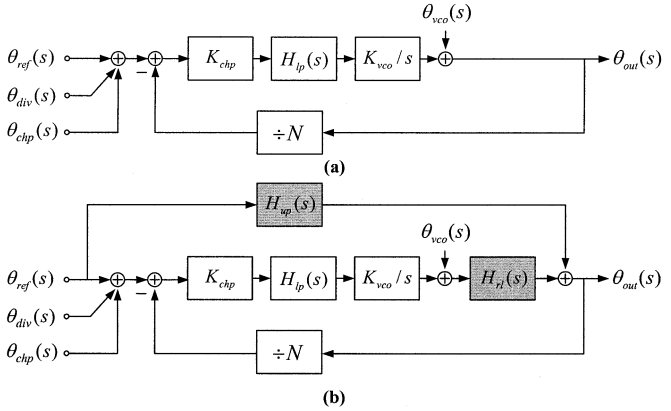

Fig. 6. (a) Commonly used phase noise model of a conventional integer-N PLL. (b) Modified version of the phase noise model describing the RPLL: the realignment adds an extra signal path from the reference to the VCO; the input noise has a different transfer function from the reference noise.

(9)–(11) can be applied to replace the phase noise from the VCO without realignment, $\theta_{\text{vco}}(s)$, with that of the realigned VCO, $\theta_{\text{inst\_vco}}(s)$. The resulting model, shown in Fig. 6(b), describes the output phase noise from the RPLL. Unlike in the conventional PLL, the transfer function for the reference noise differs from that of the other input noise sources because of the extra signal path from the reference to the VCO.

Fig. 7 shows transfer functions derived from the linearized RPLL model for β values of 0, 0.5, and 1, which correspond to no phase realignment (i.e., a conventional PLL), partial phase realignment, and complete phase realignment, respectively. In the signal flow diagram of the linearized RPLL model, there is only one feedback loop. The phase and magnitude squared responses of the loop gain are shown in Fig. 7(a). As indicated in the figure, stronger realignment increases the phase margin of the loop gain. Fig. 7(b) shows the magnitude squared of the transfer function applied to the VCO phase noise. As indicated in the figure, the stop-band of the transfer function is effectively widened and therefore the VCO phase noise is attenuated as the strength of the realignment is increased. Fig. 7(c) shows the magnitude squared of the transfer function applied to both the divider phase noise and the charge pump phase noise. As shown in the figure, the RPLL provides significantly more attenuation of these noise sources than the conventional PLL. The transfer function applied to the reference phase noise is shown in Fig. 7(d). In contrast to the other phase noise sources, there is less attenuation of the reference phase noise as β is increased because of the second path through which reference noise power is coupled into the VCO at each realignment.

The reduced attenuation of the reference phase noise in the RPLL relative to a conventional PLL would have been a drawback if the reference had been too noisy. However, in this particular test chip, the reference signal is very clean because it is derived from a buffered version of an off-chip crystal. Within the frequency band of interest, the reference phase noise is dominated by the buffer noise, which is estimated to be below -140 dBc/Hz when running at 19.68 MHz. Therefore, the reference phase noise contribution to the overall phase noise of the RPLL is negligible compared to those of the other noise sources in the RPLL.

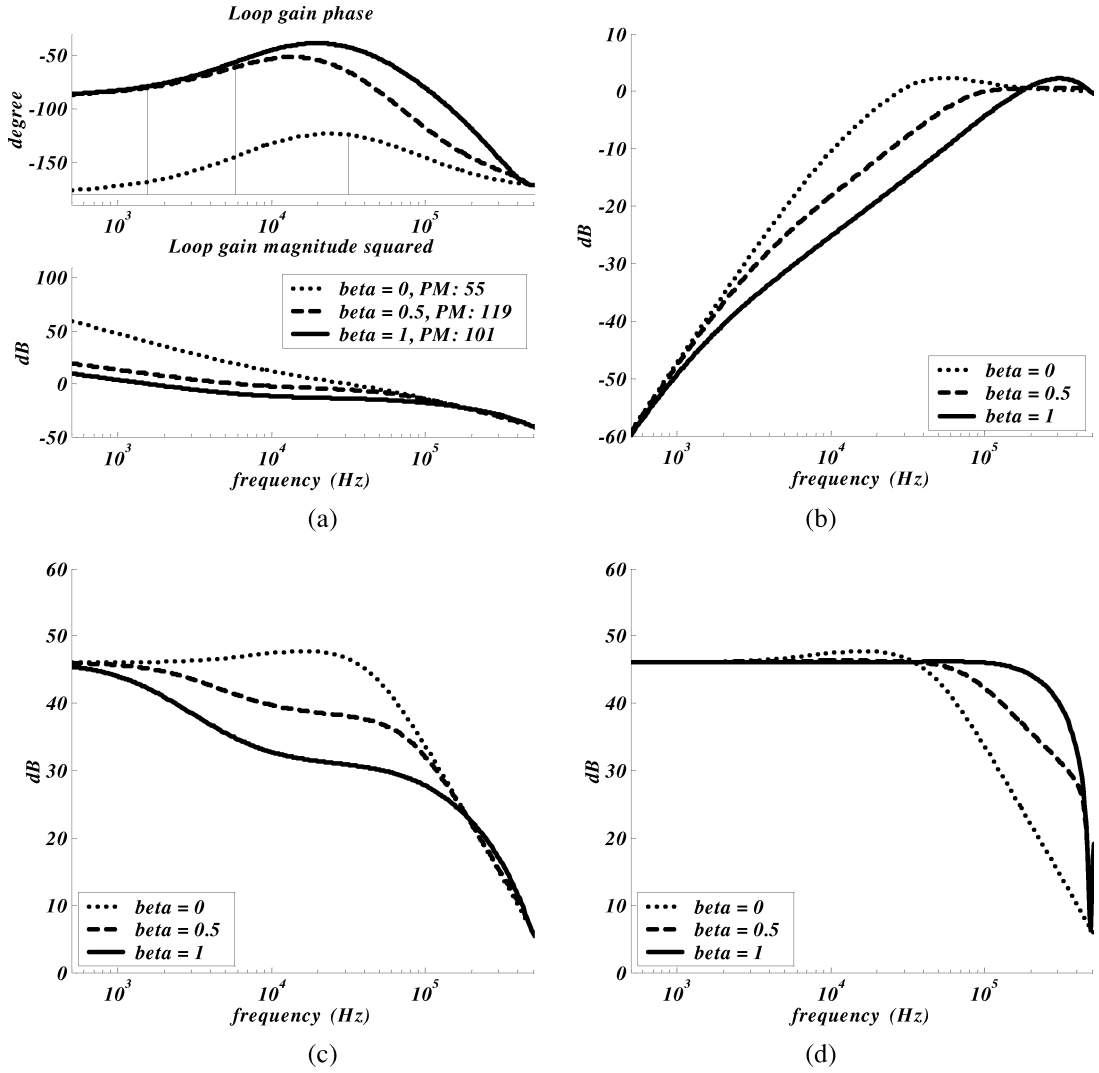

Fig. 7. Transfer function of the RPLL with different β values. (a) Loop gain. (b) VCO phase noise transfer function. (c) Divider and charge pump phase noise transfer function. (d) Reference phase noise transfer function.

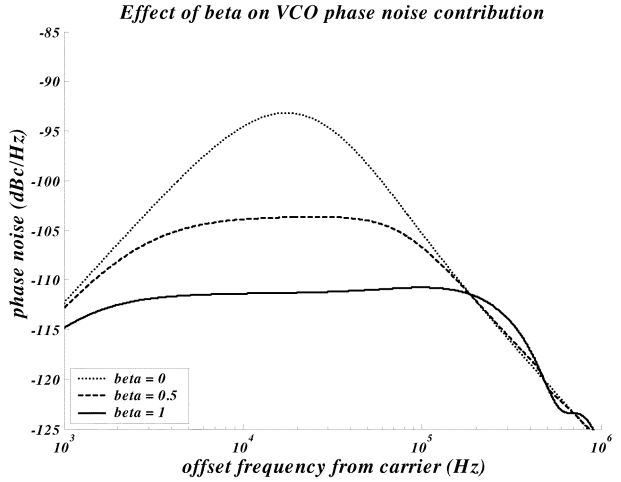

Fig. 8. Effect of β on the VCO phase noise contribution at the RPLL output.

To further illustrate the effect of β on the VCO phase noise, Fig. 8 shows the predicted RPLL output phase noise with all noise sources except the VCO set to zero and with realigning factors of $\beta = 0$, $\beta = 0.5$, and $\beta = 1$. The curves were obtained by multiplying the theoretical transfer function squared magnitude curves shown in Fig. 7(b) by the VCO phase noise PSD curve estimated from circuit simulation. As shown in the figure, attenuation of the in-band phase noise increases with β. However, the VCO phase noise power at higher frequencies increases slightly as β increases.

C. Extension of the RPLL Model to DLLs

As mentioned in the introduction, the RPLL is similar to a DLL with respect to the way it suppresses VCO noise memory. A typical DLL differs from a typical PLL in that it uses a voltage-controlled delay line (VCDL) in place of a VCO and a first-order loop filter in place of a second-order loop filter. Fig. 9(a) shows a simplified block diagram of a typical DLL [8]. Each positive-going reference edge triggers an N-tap VCDL whose individual outputs are combined to form the DLL output. The phase detector, charge pump, and the first-order loop filter adjust the VCDL such that each delay within the VCDL is equal to the reference period divided by N. Thus, when the DLL is locked, its output frequency is N times its

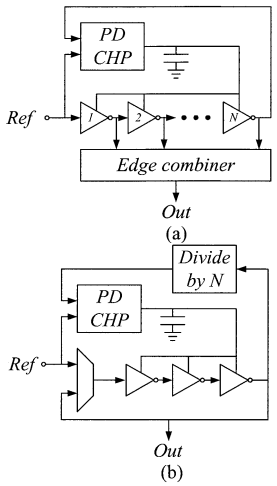

Fig. 9. (a) DLL-based clock multiplier. (b) A variant of DLL using a gated ring VCO as the VCDL.

reference frequency. A variant of this architecture is shown in Fig. 9(b) where the VCDL has been replaced by a ring VCO which can be gated on and off as shown in [9]–[11]. As in the previous DLL, each reference clock edge triggers the next N output clock edges, and the last output clock edge from the previous N cycles is discarded. Therefore, in both DLLs, noise-induced phase fluctuations are only accumulated N times. Consequently, both systems can be modeled as RPLLs for the special case $\beta = 1$.

However, in a DLL, the VCDL is characterized by the delay gain $K_{\rm vcdl}$ (s/V), while in a PLL the VCO is characterized by the VCO gain $K_{\rm vco}$ (Hz/V). The connection between $K_{\rm vcdl}$ and $K_{\rm vco}$ is illustrated as follows using the DLL example shown in Fig. 9(b). When the DLL is locked, the total delay within a reference period is $N \bullet T_{\rm vco}$. The delay gain $K_{\rm vcdl}$ is defined as the derivative of $N \bullet T_{\rm vco}$ with respect to the control voltage. As a result, $K_{\rm vcdl}$ is related to $K_{\rm vco}$ as

$$K_{\rm vcdl} = \frac{d}{dv_{\rm ctrl}} \left\{ \frac{N}{f_{\rm vco}(v_{\rm ctrl})} \right\} = -\frac{N}{f_{\rm vco}^2(v_{\rm ctrl})} K_{\rm vco} \Big|_{v_{\rm ctrl}=v_{\rm ctrl0}} \quad (12)$$

where $v_{\rm ctrl0}$ is the control voltage such that $N \bullet T_{\rm vco}$ equals one reference period.

Therefore, the previous analysis for the RPLL can serve as a universal model for DLLs and RPLLs. As demonstrated by the results shown in Fig. 7(a), the realignment increases the loop gain's phase margin, which allows the DLL to maintain stability with a first order loop filter.

IV. Implementation and Measurement Details

A. Circuit Implementation and Fabrication Issues

The prototype IC was fabricated in a 0.35-μm BiCMOS SOI process, although only CMOS components were used to facilitate later migration to a CMOS process. The process incorporates a low-resistivity buried epilayer, that, in the case of the prototype, forms a single island over which the entire circuit lies. As a result of parasitic capacitances associated with the buried epilayer, the electrical characteristics of the individual circuit components are comparable to those of a 0.6-μm standard CMOS process.

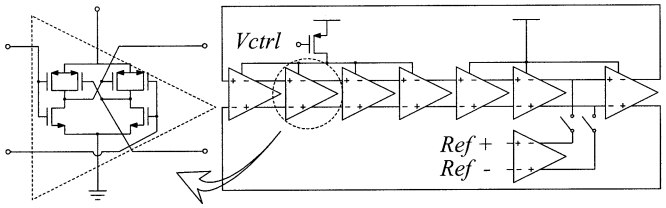

Fig. 10. Simplified circuit diagram of the realigned ring oscillator in prototype.

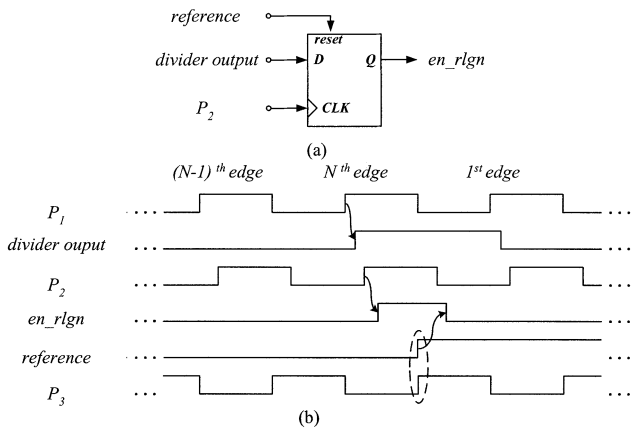

Fig. 11. Simplified timing diagram of the realignment control logic block. (a) Simplified block diagram of the realignment control logic block. (b) Timing diagram of the generation en_rlgn.

The details of the VCO and realignment circuitry represent the primary differences between the RPLL implementation and that of a conventional PLL. A simplified circuit diagram of the implemented VCO is shown in Fig. 10. It is a seven-stage ring oscillator in which four of the inverters are used to control the frequency and three introduce a fixed delay. This separation was made to minimize charge injection from the realignment switches into the sensitive VCO control node. Although not shown in the figure, the supply voltage on the fixed inverters is level shifted to 1.5 V so as to approximately match the drain voltage of the VCO frequency control transistor. The pseudo-differential topology was used to achieve high common mode noise rejection.

The control logic block generates a voltage pulse signal en_rlgn which creates a time window surrounding each instant at which a buffered reference edge and a VCO edge ideally coincide. The control logic block is enabled only when the PLL is locked in which case the VCO internal edge is close to the buffered reference edge. Fig. 11(a) shows a simplified diagram of the control logic block where the logic core is just a D-flip-flop with reset. Fig. 11(b) shows a detailed timing diagram associated with the generation of en_rlgn. Three internal VCO delay cell outputs, denoted P_1, P_2, and P_3, facilitate the generation of en_rlgn. The P_1 signal is used to drive the divider, the P_3 signal is realigned to the reference, and the P_2 signal slightly precedes P_3. The Nth rising edge of P_1 triggers the rising edge of the divider output. Then the next rising edge of P_2 samples the divider output. Since P_2 precedes

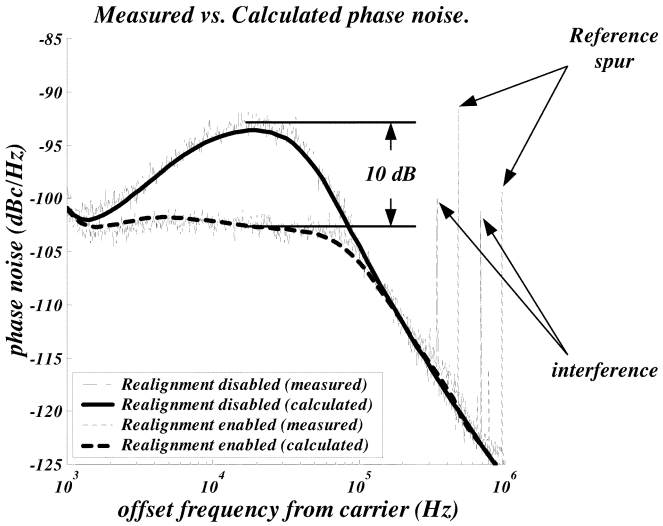

Fig. 12. Measured and calculated phase noise PSD plots for the PLL with realignment enabled and disabled. (PLL bandwidth = 32 kHz.)

P_3, it ensures that en_rlgn rises before P_3. Once the reference edge finishes rising, the phase realignment is complete, so the rising edge of the reference is used to trigger the falling edge of the en_rlgn signal, thereby disconnecting the buffered reference from the VCO.

Conventional techniques were used for most of the other circuit blocks in the system. The charge pump is similar in topology to that used in [12] with an op-amp feedback circuit to facilitate matching of the up and down currents. The phase-frequency detector is a dual D-flip-flop structure with a delay inserted in the reset path to eliminate the dead zone. The divider is asynchronous with a D-flip-flop to resynchronize the output to the VCO signal so as to reduce the noise contribution from the divider circuitry.

B. Calculated and Measured Phase Noise PSD Plots

Fig. 12 shows representative measured and calculated PSD plots of the PLL phase noise with the realignment technique enabled and disabled for the case of a 19.68-MHz crystal. Similar results were observed for the other crystal frequencies. The case shown corresponds to a reference frequency of 19.68 MHz $\div$ 41 = 480 kHz, $N = 200$, a charge pump current of 1 mA, a VCO gain of 136 MHz/V, and a loop filter consisting of a 6.8-nF capacitor in parallel with a series combination of a 330-Ω resistor and a 68-nF capacitor. The resulting PLL bandwidth is 32 kHz. As can be seen from the figure, the realignment technique causes a significant reduction in the power of the phase noise as expected, and the calculated PSD plots are in close agreement with the measured PSD plots.

The calculated PSD plots were obtained by applying the transfer functions deduced from the theoretical model to measured PSD plots of the reference phase noise and free running VCO phase noise. The free-running VCO phase noise PSD was determined by narrowing the PLL bandwidth and measuring the resulting PLL phase noise PSD, because beyond the PLL bandwidth the phase noise is dominated by the VCO phase noise. Conversely, the reference phase noise PSD was determined by measuring the PLL phase noise PSD with a very wide PLL bandwidth. In applying the theoretical model, a value of $\beta = 0.52$ was used. This is the value obtained from transistor level simulations using the nominal process corner simulation models at room temperature. Although the value of β varies across process corners and with temperature, simulations indicate the variation in β only translates into about a $\pm$1.5-dB variation in the in-band spot phase noise.

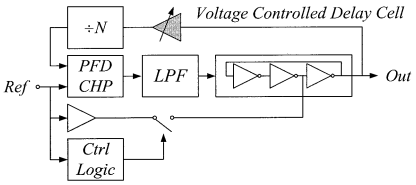

Fig. 13. Reference spur reduction with delay mismatch cancellation.

C. The Realigning Factor Revisited

The value of β deserves further explanation as it is crucial in the VCO phase noise suppression. Observed in "isolation," the realigned clock edge is driven by both the VCO delay cell and the reference buffer. Since it is desirable to completely correct the VCO phase error, the reference buffer was designed to be five times larger than the VCO delay cell in the prototype chip. Consequently, the buffer overrides the VCO and the realigned edge is dragged to be almost in phase with the buffered reference. Therefore, intuitively, one would expect β to be close to 1 in the prototype, and, indeed, this would have been the case if the delay cells in the VCO behaved as independent edge-triggered inverters. However, in practice, the perturbation from the realignment stage inevitably affects the remaining delay cells through the shared tail current source, and the value of β is reduced by the cross coupling between the delay cells. Circuit simulations indicate that β can be increased to 0.9 if better tail current source isolation is used to reduce the coupling between the delay cells. Unfortunately, this phenomenon and the attendant reduction in β were discovered during the testing phase of the prototype chip, so no experimental results are available for verification of the assertion that β can be increased through improved delay cell isolation. Interestingly, the DLL, which ideally has a β of 1, is not immune to the realignment perturbation problem. Even in a DLL care must be taken to isolate the delay cells. Circuit simulations indicate that a carefully designed DLL with a similar topology to that shown in Fig. 9(b) and VCO inverters as shown in Fig. 10 only gives $\beta = 0.5$. Evidently, in applications where a high β value is desired, great care must be taken properly to isolate the delay cells.

D. The Reference Spur Issue

In a conventional PLL, there is only one phase comparison between the VCO phase and the reference phase, and this occurs at the phase-frequency detector. In the RPLL, however, an extra phase comparison is performed at the phase realigning point, so there are two signal paths from the reference to the VCO output. In practice, mismatches between the two reference signal paths increase the power of the reference spur in the PLL output. In the prototype chip, the measured reference spur power is -34 dBc with the realignment technique enabled, and -78 dBc with

TABLE I
PERFORMANCE SUMMARY

Technology	**0.35 μm BiCMOS SOI (with only CMOS components used)**
Supply voltage	**2.7-3.3V (measurements at 3V)**
Total power consumption	**6.8mW (no observable difference when realignment enabled)**
Die size	**1.8 mm^2**
RPLL core area	**0.22 mm^2. Conventional PLL: 73% Realignment circuitry: 27%**
Spot noise @ 20 kHz offset (32kHz PLL bandwidth)	**-92.5 dBc/Hz (realignment disabled) -102.5 dBc/Hz (realignment enabled)**
Reduction of integrated noise power from 1 kHz - 50 kHz	**8.3 dB with 32 kHz PLL bandwidth 5.3 dB with 50 kHz PLL bandwidth**

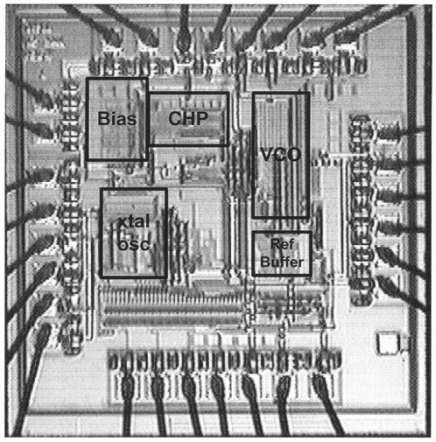

Fig. 14. Die photo of prototype chip.

the realignment technique disabled. While not a major concern in the application for which the prototype was designed, the increased reference spur power may be a drawback in other applications. In anticipation of the possible future inclusion of an automatic path calibration loop, a variable delay element has been included in the prototype prior to the divider to allow for such calibration as shown in Fig. 13. With this feature enabled and manually calibrated, the measured spur power is -71 dBc and static, which suggests that an automatic calibration loop, if necessary, would be effective. In such a control loop, the delay mismatch of the two signal paths would be detected by a phase detector with the resulting phase error lowpass filtered and fed to the voltage controlled delay cell to compensate for the mismatch. The variable delay cell introduces a nominal delay of 3 ns to the loop, which is comparable to the frequency divider delay and negligible compared with the reference period. Therefore, the extra delay has negligible effect on the loop stability.

The spurs visible in Fig. 12 that are not harmonics of the reference were caused by interference from external equipment. The evidence for this conclusion is that the power levels and frequencies of the spurs changed over time.

E. Performance Summary

The measured performance of the prototype IC is summarized in Table I. The realignment technique reduces the peak in-band phase noise by 10 dB and reduces the phase noise integrated from 1 to 50 kHz by 8.3 dB. With the loop bandwidth increased to a less conservative 50 kHz, which is near the maximum value prior to instability under nominal process conditions at room temperature, the integrated phase noise improvement changes from 8.3 to 5.3 dB. The total measured power dissipation of the IC is 6.8 mW from a 3-V supply with no observable difference when the realignment technique is disabled. A die photograph of the fabricated circuit indicating the major functional blocks is shown in Fig. 14.

V. CONCLUSION

A VCO realignment technique applied to a conventional integer-N PLL to reduce the phase noise contribution from the VCO has been proposed. A theoretical model for the new PLL that builds upon the well-known conventional PLL linearized model has been developed. Implementation details of and measured results from a CMOS reference PLL with a ring VCO capable of converting most of the popular crystal reference frequencies to a 96-MHz RF PLL reference and baseband clock for a direct conversion Bluetooth wireless LAN have been presented and used to demonstrate the technique. The measured results are in close agreement with those predicted by the theoretical model, and demonstrate that the realignment technique results in a significant phase noise reduction.

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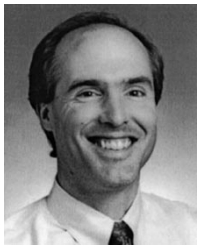

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