A 12-mW ADC Delta–Sigma Modulator With 80 dB of Dynamic Range Integrated in a Single-Chip Bluetooth Transceiver

Jorge Grilo, *Member, IEEE*, Ian Galton, *Member, IEEE*, Kevin Wang, *Member, IEEE*, and Raymond G. Montemayor, *Associate Member, IEEE*

***Abstract*—This paper presents a switched-capacitor multibit *ADC* delta–sigma modulator for baseband demodulation integrated in a single-chip Bluetooth radio-modem transceiver that achieves 77 dB of signal-to-noise-plus-distortion ratio (SINAD) and 80 dB of dynamic range over a 500-kHz bandwidth with a 32-MHz sample rate. The 1-mm^2 circuit is implemented in a 0.35-μm BiCMOS SOI process and consumes 4.4 mA of current from a 2.7-V supply.**

***Index Terms*—Data converters, delta–sigma modulators, mismatch noise shaping, wireless receiver.**

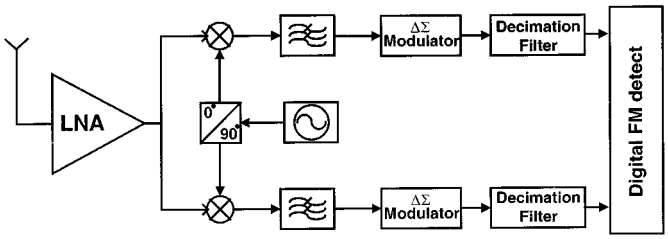

Fig. 1. Bluetooth receiver topology.

I. Introduction

MANUFACTURERS of mass-market battery-operated digital wireless transceivers such as cellular telephone handsets and wireless LANs face significant market pressures, both to avoid the use of off-chip analog filters and to reduce current consumption. Direct downconversion receivers are promising in these respects, because they minimize the use of off-chip filters and allow much of the signal processing to be performed efficiently in the digital domain [1]–[3]. By converting the received signal band directly to baseband, they allow most of the channel filtering to be performed by low-pass filters which are amenable to on-chip implementation. Since analog low-pass filters with high selectivity and linearity tend to be more power hungry than comparable digital filters, a particularly efficient option is to use digital filters for the bulk of the channel filtering with analog filtering relegated primarily to anti-aliasing [1]. This approach has been proven effective in low data-rate radios such as cellular telephones, but it is more difficult in higher data-rate applications such as Bluetooth, HomeRF, and IEEE 802.11, because of the greater burden placed on the baseband ADCs. Nevertheless, as demonstrated by this work, it is possible to design low-power ADCs with sufficient bandwidth and dynamic range for the approach to be beneficial in a Bluetooth receiver.

Specifically, the paper presents the details of a pair of low-power ADC $\Delta\Sigma$ modulators for in-phase and quadrature demodulation in a single-chip Bluetooth radio-modem transceiver [4]. Each $\Delta\Sigma$ modulator has an input sample rate of 32 MHz and achieves 80 dB of dynamic range over the Bluetooth baseband bandwidth of 500 kHz. The $\Delta\Sigma$ modulators are followed by digital comb filters which, in addition to removing out-of-band quantization noise, perform most of the required channel filtering prior to frequency detection. Each $\Delta\Sigma$ modulator dissipates 11.9 mW of power, which is significantly lower than the power dissipated by other ADCs of similar dynamic range and bandwidth known to the authors [5]. Under certain scaling assumptions, it is also possible to compare the power dissipation of the $\Delta\Sigma$ modulator to those of previously reported $\Delta\Sigma$ modulators with different bandwidths and dynamic ranges. For example, under the conservative assumption that the power dissipated by a $\Delta\Sigma$ modulator increases linearly with the signal bandwidth, the only $\Delta\Sigma$ modulator known to the authors with comparable power dissipation is that presented in [6]. As shown later in the paper, the combination of high dynamic range and low power dissipation results largely from the use of a low-order $\Delta\Sigma$ modulator with multibit quantization and a BiCMOS process. The multibit quantization is made feasible by mismatch-shaping DACs modified from those presented in [7] so as to reduce processing latency.

II. Bluetooth Receiver Architecture

Fig. 1 shows a high-level view of the Bluetooth receiver topology. After low noise amplification and quadrature downconversion, the in-phase and quadrature baseband signals pass through an anti-aliasing filter and then through a second-order multibit switched-capacitor ADC $\Delta\Sigma$ modulator, followed by a comb decimation filter. The 32-MHz sample rate represents an oversampling ratio of 32 relative to the desired Bluetooth signal, so low-order analog filters suffice for anti-aliasing filtering purposes. Much of the overall signal processing,

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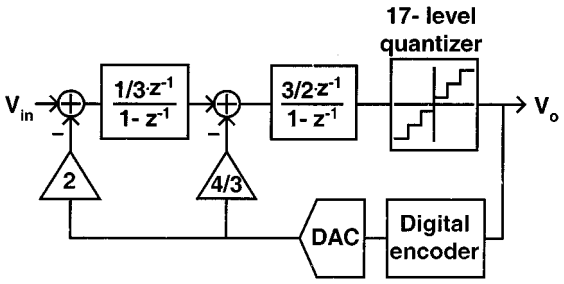


Fig. 2. Simplified block diagram of the $\Delta\Sigma$ modulator.

including channel filtering, frequency demodulation, and clock and data recovery, is performed in the digital domain.

III. Delta–Sigma Modulator Topology

A. Comparison of Different Architecture Candidates

Fig. 2 shows the simplified block diagram of the $\Delta\Sigma$ modulator. It is a second-order structure with two delaying discrete-time integrators and a 17-level quantizer surrounded by two feedback loops [8]. With ideal components and a sample rate of 32 MHz, it has a dynamic range of 87 dB over the 0–500-kHz frequency band.

The use of a low-order $\Delta\Sigma$ modulator with multibit quantization made possible the low current consumption and high dynamic range achieved by the circuit. Although a higher order single-loop architecture with one-bit quantization or a MASH architecture could have been used instead, as outlined in this section, such solutions would have resulted in higher current consumption.

To maintain stability with one-bit quantization, the pole and zero placement in single-loop high-order $\Delta\Sigma$ modulators is highly constrained. This generally results in less aggressive quantization noise shaping, thereby necessitating higher order loops, and a lower input no-overload range than is possible with multibit quantization. For instance, to achieve the necessary in-band dynamic range for the given frequency plan and application described in this paper, a sixth-order $\Delta\Sigma$ modulator, typically requiring six opamps, would have been necessary [9]. The lower input no-overload range generally necessitates larger input sampling capacitors to achieve a given signal-to-thermal-noise ratio, and this gives rise to opamp designs with greater current consumption.

MASH structures became popular for high-dynamic range applications because they facilitate higher order $\Delta\Sigma$ loops that do not suffer from stability problems. However, they rely on good matching between analog and digital transfer functions; in the presence of mismatches, quantization noise from the front-end stages appears at the output. Moreover, these structures are characterized by an inherent loss in dynamic range due to internal signal scaling. These two factors impose constraints on the minimum size that can be used for capacitors, and hence on the minimum current consumption that can be achieved. A popular structure consists of a second-order single-loop modulator followed by a first-order modulator. Although practical, the structure requires three opamps, and the last stage opamp sums three input signals, thereby increasing its capacitive load, and hence its current consumption.

In contrast, the multibit second-order architecture used in the circuit presented here requires only two opamps. Furthermore, its no-overload range is nearly equal to its reference voltage, which allows for smaller input sampling capacitors compared to the other architectures, and hence opamps with lower current consumption. As described in the next section, the architecture does require a significant amount of digital logic to implement the mismatch-shaping DACs, but the current consumed by this logic is small compared to the current consumed by the rest of the circuit. This trend is further supported by migration to small feature processes.

IV. Circuit Design

A. Switched-Capacitor Top-Level Design

Fig. 3 shows the simplified circuit schematic of the modulator. To accommodate a low power supply voltage with good sampling switch performance, the input common-mode voltage V_{cmi} of the operational amplifiers was set at 1 V. This low value permitted the use of small, single n-channel devices for accurate definition of the sampling time.

The design uses a negative reference voltage, that is, $V_{\rm refm} = V_{\rm cm} - V_{\rm ref}$, where the common-mode voltage $V_{\rm cm} = 1.35$ V and $V_{\rm ref} = 0.7$ V. This allows the use of small sampling switches and results in low reference noise power (11 $\mu V_{\rm rms}$). The reference voltage is derived from a resistive division of a bandgap voltage reference circuit. Since the reference value is small, the noise due to the resistors is low. To reduce the effect of signal-dependent charge injection onto the reference and charge injection due to component mismatches, a cross-sampling scheme was used. Moreover, delayed clock phases were used where appropriate.

The scaling coefficients were chosen in order to meet three main objectives. The first objective was to confine the internal signals to the high-gain, most linear region of the amplifiers. The second objective was to comply with the input common-mode requirements of the comparators in the internal flash ADC. These, too, imposed restrictions on the maximum signal swing allowed at the output of the second integrator. The third objective was to provide optimum, equal loading conditions for the first opamp in both clock phases in conjunction with a suitable choice of the input capacitor size. A factor that determined the final value of the input capacitor was kT/C noise power, in particular the partition of noise contribution within the ADC toward the total noise power budget. The total integrated kT/C noise (0–500 kHz) arising from the switches on-resistance is 45 $\mu V_{\rm rms}$, resulting in about 3-dB degradation of the noise floor when added to the quantization noise.

The output of the second integrator is sampled and quantized into a 17-level representation. The quantizer produces a 16-bit thermometer code output, which is supplied to the feedback mismatch noise shaper digital encoder for further processing, and then to the feedback DACs. A binary encoder also converts the thermometer code to a more convenient 5-bit digital representation. The output of this binary encoder constitutes the "output" of the $\Delta\Sigma$ modulator, and is fed to a decimation filter for removal of out-of-band noise, and then to a GFSK demodulator.

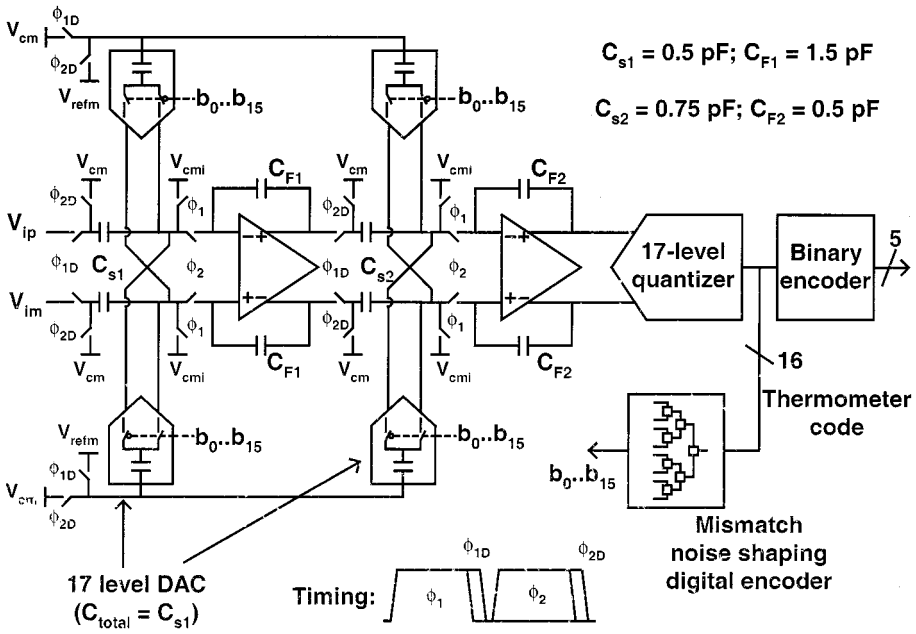


Fig. 3. Simplified circuit diagram of the $\Delta\Sigma$ modulator.

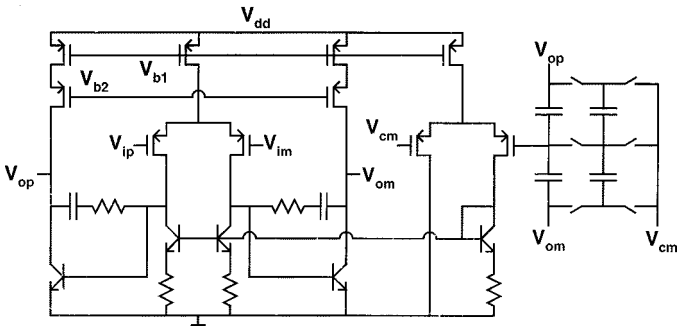


Fig. 4. Simplified opamp schematic.

Four identical DACs were used in the feedback path, each with 16 unit capacitors, with a total capacitance equal to the value of input capacitor (0.5 pF). The use of two DACs to implement the feedback path effectively realizes a coefficient of two, necessary for loop stability and for the noise shaping function. Although the inner loop feedback DAC total capacitance could be made smaller, its value was also constrained by the equal loading requirement for the first opamp. The total capacitance in the inner DAC and the second-stage scaling coefficients determine the load of the first opamp during the sampling phase.

B. Operational Amplifier

Fig. 4 shows the circuit diagram of the operational amplifier. To take advantage of the availability of bipolar devices, a two-stage Miller-compensated configuration was chosen. Using bipolar devices in the second stage results in ease of phase compensation at very modest current levels. (In an all-CMOS design, the second stage is typically notorious for consuming excessive current to achieve suitable phase margin.) A two-stage opamp is also more amenable for low-voltage design [10].

Conforming to a low value of the input common-mode voltage, the input stage of the amplifiers employed p-channel devices, with the added benefit of lower $1/f$ noise. However, the latter aspect of the design did not receive much importance, as GFSK demodulation de-emphasizes low frequency noise. Moreover, the hopping frequency in Bluetooth is 1.6 kHz, and hence no significant energy exists below that frequency. (This applies for DH1 packets. For DH5 packets, the hopping frequency can be as low as 533 Hz; however, DH5 packets imply large signals, and sensitivity is not an issue.) The simulated integrated opamp noise in the band (1–500 kHz) was 20 $\mu V_{\rm rms}$, making it the main noise contributor (60%).

The opamp was designed to have a dc gain of 80 dB, a unity-gain frequency of 350 MHz, and a phase margin of 80°, in both clock phases. The amplifier uses a conventional switched-capacitor network to set the output common-mode voltage at 1.35 V.

C. Comparator Used in the Flash ADC

Fig. 5 shows the circuit diagram of the comparators used in the internal flash ADC. The use of bipolar devices at the input stage resulted in a design with low input-referred offset, at low current levels. This is attributable to the inherently low offset of the bipolar devices, and to their large transconductance, relative to that of the p-channel load devices. The estimated standard deviation of the input-referred offset is 4 mV.

The comparator structure employs resetting to reduce hysteresis. In particular, during phase ϕ_2 the outputs are shorted to ground, and hence it is necessary for proper operation of the modulator to hold the outputs for a full clock cycle. For that purpose, the topology requires static latches at the output. Such latches, however, were not used at this point for reasons that will be addressed later in the paper.

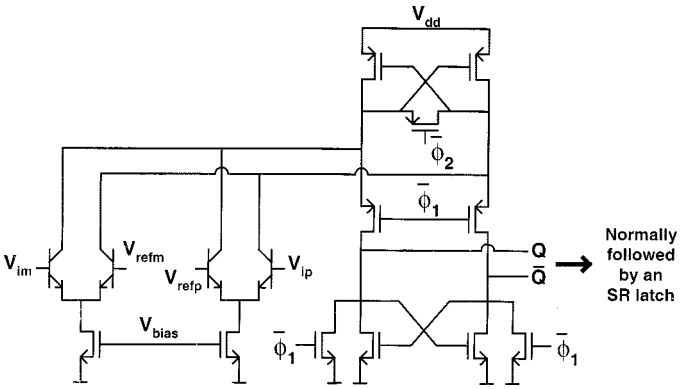


Fig. 5. Comparator used in the internal flash ADC.

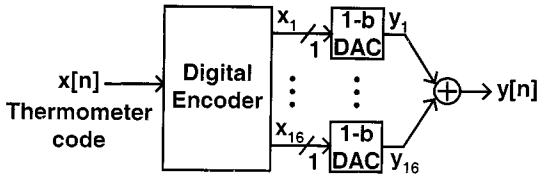


Fig. 6. Generalized block diagram of a 17-level DAC.

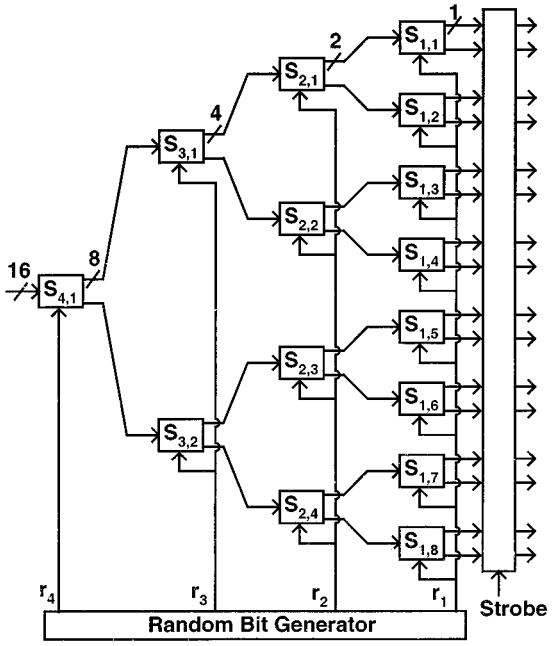
D. The Feedback Path

Fig. 6 shows a simplified block diagram of a generalized 17-level digital-to-analog converter. It consists of a *digital encoder* followed by a bank of 16 one-bit DACs whose analog outputs are summed to generate the overall output, $y[n]$. The input sequence, $x[n]$, is restricted to the set $\{-8, -7, 8, 8\}$. During each sample interval the digital encoder sets $8 + x[n]$ of its output bits high and $8 - x[n]$ of its output bits low. Each one-bit DAC generates an analog output given by $1/2 + e_{hi}$ if its input bit is high, and $-(1/2) + e_{li}$ if its input bit is low, where e_{hi} and e_{li} are the high and low one-bit DAC errors, respectively. The DAC errors are assumed to result primarily from static component mismatches. Thus, if there were no mismatches, the output of the DAC would be $x[n]$. As shown in [11], in this case the overall DAC output has the form

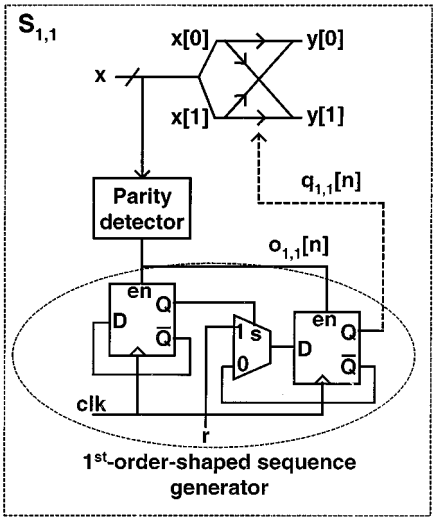
$$y[n] = \alpha \cdot x[n] + \beta + e_{\mathrm{DAC}}[n]$$

where α is a constant gain, β is a constant offset, and $e_{\mathrm{DAC}}[n]$ is *DAC noise* that depends upon the input sequence and the one-bit DAC errors in general. The purpose of the digital encoder is to cause $e_{\mathrm{DAC}}[n]$ to be white or spectrally shaped as required by the application. For the present application, the digital encoder is designed to suppress the power of the DAC noise in the frequency band below 500 kHz, so it is referred to as a mismatch noise shaping digital encoder.

The mismatch noise shaping digital encoder consists of digital logic blocks, called *switching blocks*, organized in a tree structure as shown in Fig. 7(a) [11]. Each switching block partitions its input sequence into two output sequences according to a prescribed algorithm. Fig. 7(b) shows the details of the $S_{1,1}$ switching block. It contains a swapper cell that permutes the input bits according to the value of the kth bit in the sequence $q_{1,1}[n]$. This sequence is a function of the input signal through



(a)



(b)

Fig. 7. (a) Mismatch noise shaping digital encoder. (b) Implementation details of the $S_{1,1}$ switching block.

a parity detector, and some additional processing. As shown in [7] and [11], this configuration results in a distortion component given by

$$e_{\mathrm{DAC}}[n] = \sum_{k,r} (\text{constant}) \cdot q_{k,r}[n]$$

where

$$q_{k,r}[n] = \begin{cases} 0, & \text{if } o_{n,r}[n] = 0 \\ 1, & \text{if } o_{n,r}[n] = 1 \text{ and } q_{n,r}[n] = 1 \\ -1, & \text{otherwise.} \end{cases}$$

Therefore, the DAC noise inherits the properties of the switching sequences, $q_{k,r}[n]$. It can be shown that the circuit consisting of two flip-flops shown in Fig. 7(b) generates a

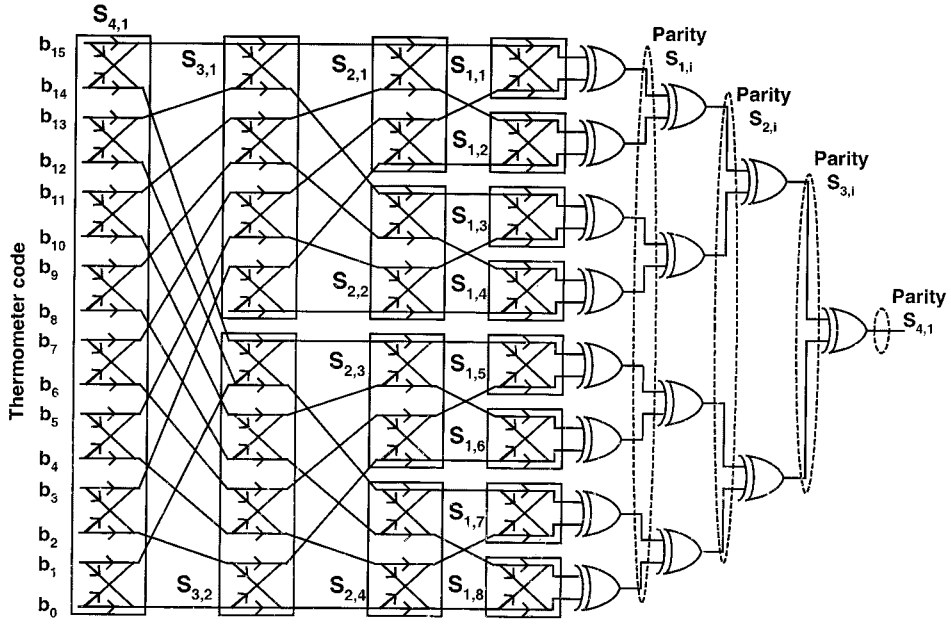


Fig. 8. Connection of the swapper cells and parity detection.

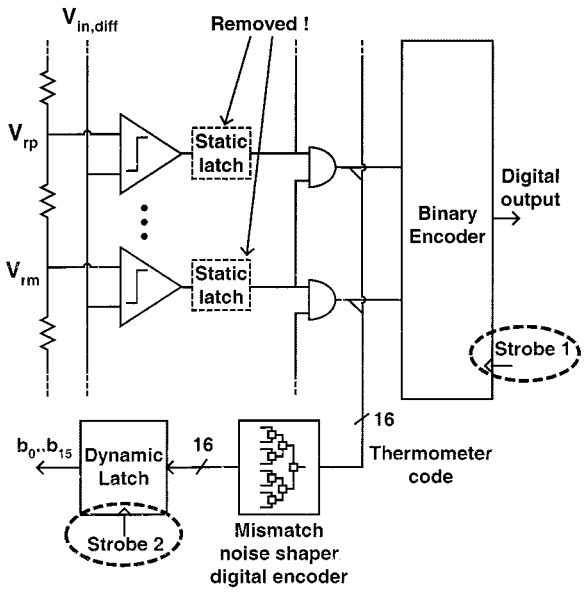


Fig. 9. The shift of the latching function with the purpose of reducing latency.

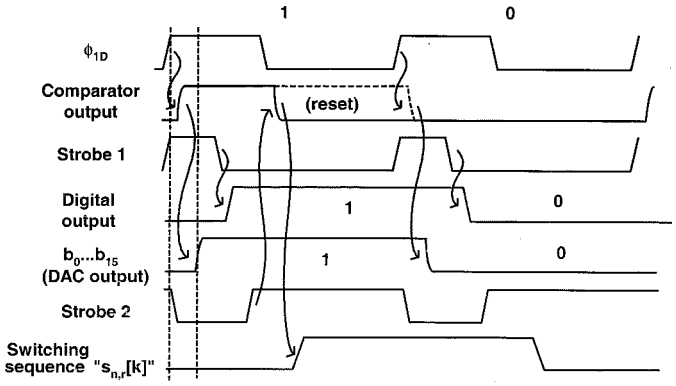


Fig. 10. Timing diagram.

sequence whose integral is bounded, which is a sufficient condition for the power spectral density to be zero at dc, which for this case implies first-order high-pass spectral shaping. Hence, the DAC noise is also first-order noise shaped. (Analogously, Nth-order noise shaping can be achieved by generating sequences whose Nth integral is bounded.)

All mismatch noise shaping digital encoders suffer from the inherent shortcoming that they introduce additional delay to the overall DAC. The delay increases linearly with the number of bits, which can be particularly problematic in high data rate systems. For proper operation, the signal must propagate around the feedback loop in a period of time much shorter than half a clock cycle or it will generate glitches that disturb the settling of the amplifiers. In contrast, the parity detection mechanism does not have to be fast, as the information generated in one clock cycle is used only during the next one.

To reduce the latency through the mismatch noise shaping digital encoder, the swapper cells were implemented with minimum-size CMOS transmission gates. Although the resulting switching blocks perform the same mathematical operations as those presented in [7], the use of transmission gates instead of conventional digital logic allowed a significant reduction in the propagation delay. The parity detection was done *a posteriori*, in the following clock cycle, utilizing an inverted tree of XOR gates whose outputs contain the parity information to be used in their respective layers (Fig. 8). To further reduce the latency through the feedback loop, the latching function required to hold the output of the flash ADC comparators for a full clock cycle was moved to the outputs of the mismatch noise shaping digital encoder and binary encoder (Fig. 9). These measures facilitated a reduction of the propagation delay between the clock edge that commands the update of each comparator output in the ADC and the corresponding edge at the output of the feedback DACs to 1 ns. Fig. 10 shows the timing diagram of critical events.

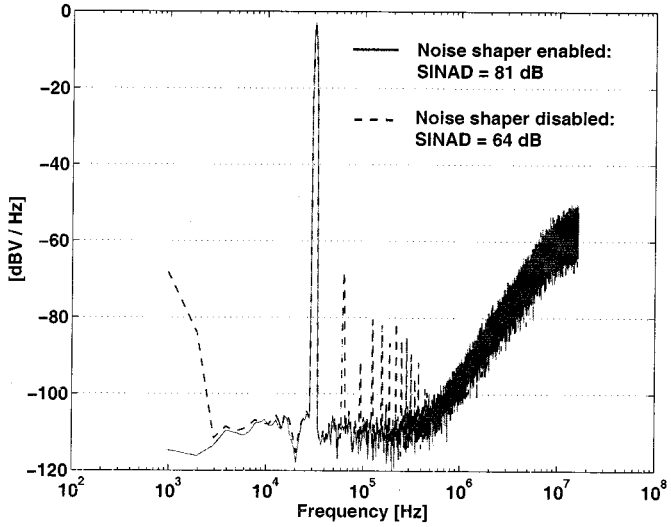


Fig. 11. Simulated output spectrum when the mismatch noise shaper is enabled and disabled.

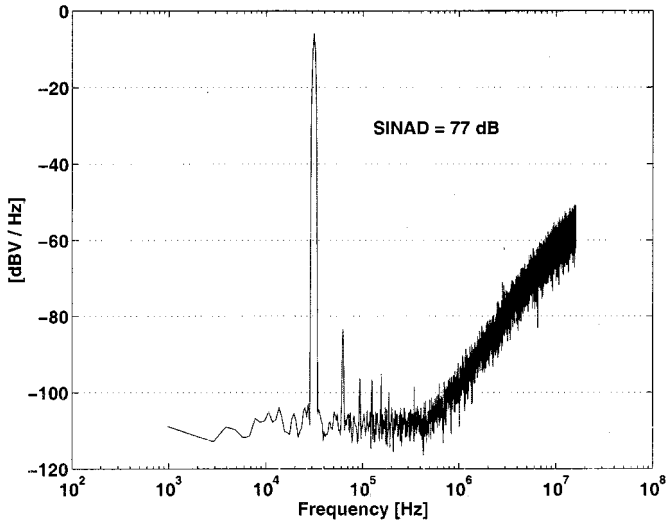


Fig. 12. Measured output spectrum.

E. Simulated Results

Fig. 11 shows the simulated output spectrum of the modulator for a 1.31 $V_{p,diff}$, 31.25-kHz sinusoidal input signal, using an estimated 0.3% matching among the feedback DAC elements. Also shown is the result of disabling the mismatch noise shaper digital encoder, with the same simulation parameters. While the former achieves a peak signal-to-noise-plus-distortion ratio (SINAD) of 81 dB, the latter is limited to about 64 dB due to harmonic distortion. This figure clearly demonstrates the effectiveness of the technique. The simulation included the equivalent input-referred noise due to the opamp, kT/C, and reference noise.

V. Experimental Results

Fig. 12 shows the measured output spectrum, which can be compared with the simulated results in Fig. 11. The signal applied possessed the same amplitude and frequency as the one used in simulations. The peak SINAD is only 77 dB, rather than 81 dB, which is attributable mostly to a certain degree of current starvation in the opamps and offsets in the flash ADC. The noise floor is in agreement with the simulated result. Although not shown, disabling the mismatch noise shaper digital encoder produced results within 2 dB of the simulation, supporting the earlier estimation of capacitor mismatches.

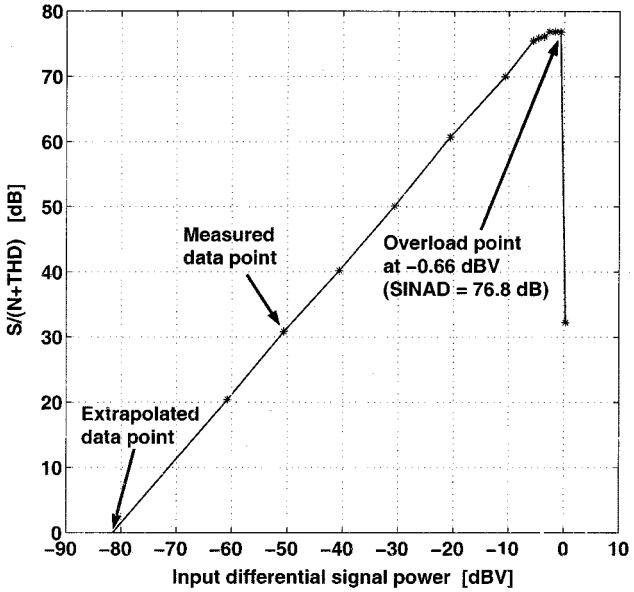


Fig. 13. Measured signal-to-noise-plus-distortion ratio for a 31.25-kHz sinusoidal input signal.

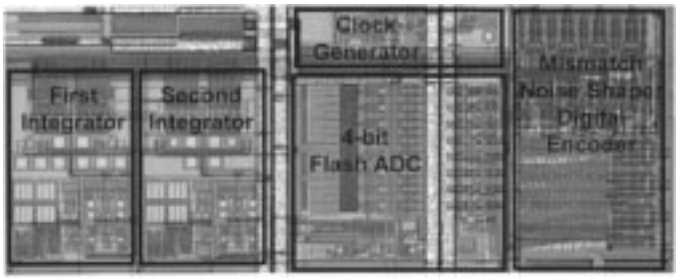


Fig. 14. Chip photograph.

Fig. 13 shows the measured SINAD again for a 31.25-kHz input signal frequency. This curve shows a dynamic range of 80 dB and a peak SINAD of about 77 dB. Note that the SINAD stops increasing linearly with the input signal power at about −6 dBV, due to the distortion mechanisms mentioned above, not due to quantization noise. Although the measurements shown here were done with a relatively low frequency input signal, no observable differences were noted for higher frequencies, both in our measurements and in system-level measurements. These measurements were done with a 2.7-V power supply, and the measured current was 4.4 mA.

Fig. 14 shows the die photograph of one channel, with indication of the location of each main block. (The second channel is a mirrored version around the bottom horizontal axis.) The total area shown is about 1 mm^2.

Table I summarizes the performance of the modulator, and Table II its current consumption breakdown. Most of the current was consumed in the analog circuitry.

TABLE I
SUMMARY OF THE PERFORMANCE OF THE MODULATOR

Signal band	0 – 500 kHz
Sampling frequency	32 MHz
Dynamic range	80 dB
Peak SINAD	77 dB
Peak SFDR	78 dB
Power supply voltage	2.7 V
Power supply current	4.4 mA
Die Area	1.0 mm^2

TABLE II
CURRENT CONSUMPTION STRUCTURE

Op-amps, bias, other analog	2.9 mA
Clock generator, digital encoder, other digital	1.0 mA
Clock buffers, other A/D interface circuits	0.5 mA

VI. CONCLUSIONS

The implementation details of a delta–sigma modulator ADC for quadrature baseband demodulation integrated in a commercial direct-conversion Bluetooth radio-modem transceiver have been presented. The design achieves 80 dB of dynamic range and 77 dB of peak SINAD over the 0–500 kHz Bluetooth signal bandwidth, with a current consumption of 4.4 mA. The low current consumption was made possible through the use of multibit quantization, which permitted the use of a low-order single-stage delta–sigma modulator with relaxed opamp requirements, and innovations in the design of the feedback path components, including the mismatch-shaping DAC logic so as to minimize latency. Judicious use of n-p-n bipolar transistors in the opamps and comparators also resulted in current savings relative to that which would likely be achieved in a comparable fully CMOS design.

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