

## 5.2 A Direct-Conversion Single-Chip Radio-Modem for Bluetooth

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The low power, low cost, and high level of integration associated with a direct-conversion architecture are ideally suited for consumer-oriented digital radio applications such as Bluetooth. However, previously-published single-chip Bluetooth transceivers all employ a low-IF receiver architecture as exemplified in Reference [1]. In contrast, this commercially-available direct-conversion single-chip Bluetooth radio-modem is well-suited for cellular applications where power consumption and blocking performance are critical. This direct-conversion architecture radio resembles a "software-defined radio," which can be directly scaled to accommodate the next-generation Bluetooth system operating at 2Mb/s, as well as other multi-mode radio applications. This chip integrates the entire analog front-end transmit and receive functions as well as the digital modem in a 0.35 $\mu$ m 27GHz  $f_r$  SOI BiCMOS technology. The SOI BiCMOS process offers good on-chip isolation from LO leakage and digital switching noise, which are especially problematic in a direct-conversion transceiver implementation.

The transceiver architecture is shown in Figure 5.2.1a. The transmitter path adapts a conventional direct-conversion approach where the digital modem (Figure 5.2.1b) generates a discrete-time GFSK modulated I-Q signals, each of which is subsequently converted into an analog waveform by a DAC followed by a low-pass reconstruction filter (LPF). Each DAC uses a charge-redistribution algorithm that is inherently area and power efficient, resulting in a total current consumption of only 2mA for both I-Q DACs and filters. The reconstructed baseband signal is up-converted by a resistively-degenerated Gilbert-type mixer with resistive loads as shown in Figure 5.2.2. The I-Q LO drive signal is derived from a 2-stage polyphase filter whose input comes from a 2.4GHz VCO locked to a 1MHz reference frequency. The power amplifier, also shown in Figure 5.2.2, consists of a single-stage open-collector differential-pair with off-chip matching and balun for maximum power transfer. A 30dB power control with 8 discrete power steps is achieved by controlling the transconductance  $g_m$  of the differential pair through a digitally controlled tail current source. This power amp is capable of delivering a +3dBm continuous tone into a 50 $\Omega$  load while dissipating 9mA. The chip also includes auxiliary circuits (not shown) such as a crystal oscillator for generating a 32MHz on-chip reference frequency, a digital regulator for the modem, a low-power digital regulator and a low-power 32kHz crystal oscillator for sleep-mode operation.

The receive architecture consists of an LNA followed by I-Q mixers to quadrature down convert the desired RF signal directly to DC. With a large input dynamic range requirement from -83dBm (sensitivity) to -20dBm (Bluetooth overload spec.), the LNA is designed with a 20dB gain control to avoid overloading the ADC. Simplified circuit diagrams of the LNA and down-conversion mixer are shown in Figure 5.2.3. The differential pair in the LNA is inductively degenerated to achieve high linearity without degrading the noise figure (NF). The gain control is accomplished by a Gilbert-type current steering scheme in which the unwanted signal current is diverted to a low-impedance supply line. The LNA has 16dB gain, 5dB NF, and -10dBm IIP3.

The down-conversion mixer consists of an inductively-degenerated transconductance stage driving a commutating mixer core.

The down-converted baseband signals pass through an anti-aliasing filter (AAF) which provides out-of-band filtering prior to a 32MHz sigma-delta ADC with 80dB of dynamic range [2]. The demodulation is accomplished digitally in the modem as shown in Figure 5.2.1b. Digital channel filtering is performed before FM detection to prevent interferers and noise from capturing the FM detector. Compared to a low-IF receiver, the direct-conversion architecture avoids power-hungry and area-intensive complex-domain (I-Q) analog band-pass filter (BPF) that typically requires a tuning circuit or an auto-calibration loop to control the filter center frequency for channel selection. Digital channel-selection filters achieve the stringent adjacent and alternate channel blocking specification while consuming less power, and are more accurate, robust, and flexible than analog implementations. Another drawback of low-IF architectures is the need to reject the image-frequency and the alternate-image blockers that fold back to adjacent and alternate channels. This is critical in an interference-limited system like the Bluetooth, where the actual required channel-blocking requirements for reliable multi-user operation often exceed the Bluetooth specifications. The implemented system achieves a blocking performance of -5dB and -40dB C/I, exceeding the Bluetooth specification of 0dB and -30dB, for adjacent and alternate channel, respectively.

A unified approach to circuit and system design help combat three well-known problems associated with direct-conversion [3]. First, DC offset accumulated through the analog front-end is removed digitally in the modem via calibration that occurs between transmit and receive slots. With Bluetooth GFSK modulation, direct capacitive coupling to remove the DC offset is not a viable option since the modulation power peaks at DC. Second, even-order distortion causes AM demodulation, and also generates a DC tone in the presence of two blocking signals, e.g. two Bluetooth modulated signals at adjacent and alternate channel locations. By using an off-chip balun and fully-differential on-chip signal paths, the receiver achieves +40dBm measured IIP2, sufficient to meet in-band distortion requirements. Third, DC offset caused by LO self-mixing of spurious LO leakage to the RF input port is calibrated out digitally. An on-chip VCO with good substrate isolation, provided by the SOI substrate, minimizes LO leakage. Dynamic DC offset is not a major problem because Bluetooth devices usually remain either physically stationary or slow moving.

Measured radio-modem performance presented in Figure 5.2.4 represents the first reported direct-conversion Bluetooth transceiver. The chip includes ESD protection circuits for all pins. Figure 5.2.5 shows transmitter performance. The blocking performance shown in Figure 5.2.6a exceeds Bluetooth specs, and does not show asymmetry caused by image interferers folding back as typically seen in an IF implementation [1]. The intermodulation result is shown in Figure 5.2.6b. The die micrograph is shown in Figure 5.2.7.

### References:

- [1] H. Darabi, et al., "A 2.4GHz CMOS Transceiver for Bluetooth," ISSCC Digest of Technical Papers, pp. 200-201, Feb. 2001.
- [2] J. Grilo, et al., "A 12 mW ADC delta-sigma modulator with 80 dB of dynamic range integrated in a single-chip bluetooth transceiver," Proc. of the CICC, San Diego, CA, pp.23-26, 2001.
- [3] A. Abidi, "Direct-Conversion Radio Transceivers for Digital Communications," IEEE J. of Solid-State Circuits, vol. 30, no. 12, pp. 1399-1410, Dec. 1995.

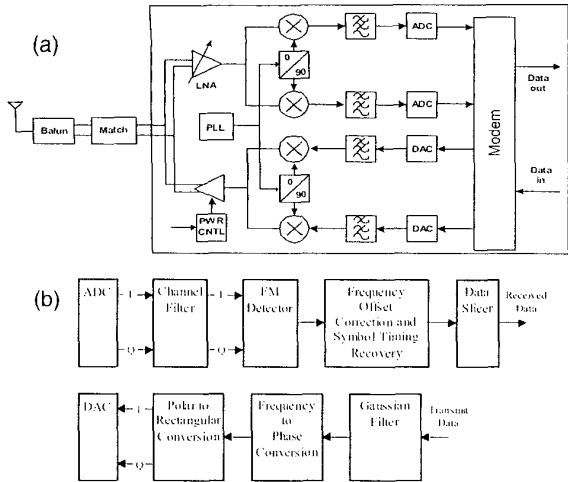


Figure 5.2.1: (a) Block diagram of the transceiver. (b) Simplified block diagram of the digital modem.

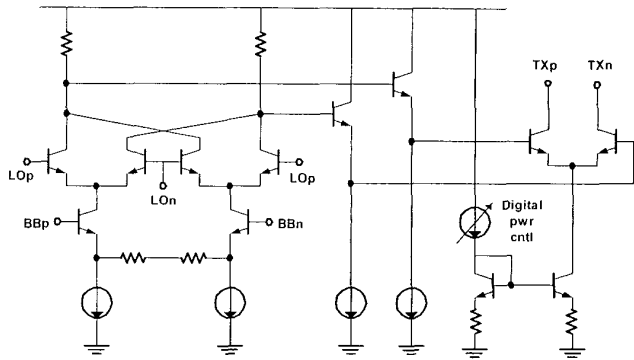


Figure 5.2.2: Circuit diagram of up-conversion mixer and power amp.

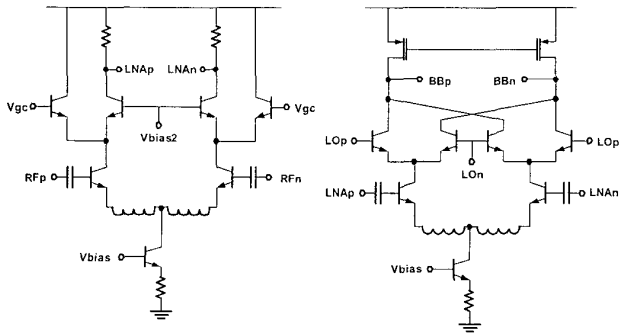


Figure 5.2.3: Circuit diagram of LNA and down-conversion mixer.

Sensitivity	-83dBm
Co-channel Blocking C/I	11dB
Adjacent-channel Blocking C/I	-5dB
Alternate-channel Blocking C/I	-40dB
RX IIP2	+40dBm
Phase noise at 3MHz offset	-123dBc
TX power output into 50Ω	+3dBm
Power supply voltage	2.7V
Analog supply current in RX mode	39mA
Analog supply current in TX mode	37mA
Digital Supply current	5mA
Sleep current	10μA
Analog core die Area	7.6mm <sup>2</sup>
Total die Area	19.5mm <sup>2</sup>

Figure 5.2.4: Measured radio-modem performance summary.

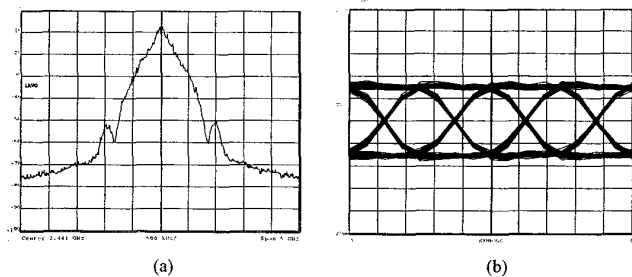


Figure 5.2.5: (a) Modulated transmitter spectrum. (b) Transmitter eye diagram.

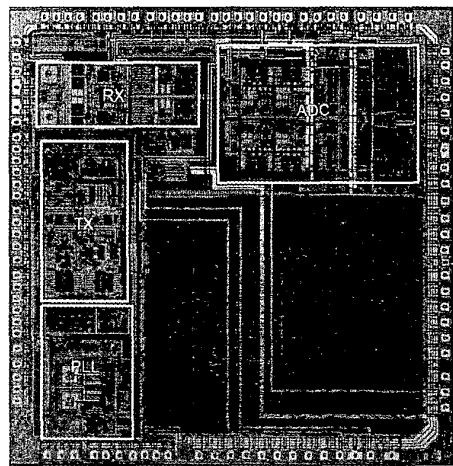


Figure 5.2.7: Die micrograph.

