A NECESSARY AND SUFFICIENT CONDITION FOR MISMATCH SHAPING IN MULTI-BIT DACS

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ABSTRACT

Mismatch-shaping digital-to-analog converters (DACs) are enabling components in most of today's high performance delta-sigma data converters. These multi-bit DACs ensure that the noise created by static component mismatches in the DAC is spectrally shaped so that most of its power resides outside of the signal band. Although most mismatch-shaping DACs adhere to a common architecture consisting of a digital encoder and a bank of 1-bit DACs, the theoretical analysis of the DAC noise has been tailored to the specific implementations. This paper presents a necessary and sufficient condition for a general multi-bit DAC to produce DAC noise that has desired properties in its PSD. As an example application, this paper uses the condition to analyze and compare several mismatch-shaping DACs.

I. INTRODUCTION

The mismatch-shaping DAC has made multi-bit $\Delta\Sigma$ modulation feasible by attenuating the signal-band portion of its resulting *DAC noise*. This noise is a consequence of the inevitable device mismatches that result from process variations in VLSI circuit fabrication and cause the multi-bit DAC to be a nonlinear device. By reducing the signal-band DAC noise, mismatch-shaping DACs have engendered most of today's high-performance $\Delta\Sigma$ data converters.

There are many mismatch-shaping DAC architectures presented in literature, but most are variants of four types: vector feedback [1], butterfly shuffler [2], tree structured [3], and data-weighted averaging (DWA) [4]. Each of the four architectures has been mathematically shown to produce DAC noise with certain desired properties in its power spectral density (PSD). The mathematics developed for the results are tailored to the specific architecture even though each DAC shares a common structure composed of a digital encoder and a bank of 1-bit DACs. Most designers have relied on these mathematics to create other architectures and have used simulations or circuit tests to show the DAC noise has the desired spectral properties, which can be misleading.

This paper provides a necessary and sufficient condition for a general multi-bit DAC to obtain DAC noise with given properties in its PSD. Unlike previous analysis for generalized DACs [5], the condition does not rely on properties of the circuit fabrication errors; the condition applies solely to the algorithm executed by the digital circuitry that enables mismatch shaping. Given a multi-bit DAC implementation, the condition can be used to evaluate whether this DAC produces DAC noise certain PSD properties. As an example of this application, this paper uses the condition to show that a lowpass implementation of each of the four previously introduced DACs produces DAC noise whose PSD is zero at dc. Additionally, this paper uses the condition to make some qualitative comparisons between the four main DAC architectures and to show that the DAC noise PSD of a lowpass architecture called partitioned DWA (P-DWA) [6] is not zero at dc.

II. THE GENERAL MULTI-BIT DAC

The general multi-bit DAC shown in Figure 1 consists of a digital encoder and a bank of N 1-bit DACs. The output of the ith 1-bit DAC is given by

$$y_i[n] = \begin{cases} \frac{\Delta_i}{2} + e_{h_i}, & \text{if } x_i[n] \text{ is high;} \\ -\frac{\Delta_i}{2} + e_{l_i}, & \text{if } x_i[n] \text{ is low;} \end{cases} \quad (1)$$

where Δ_i is the nominal step size of the ith 1-bit DAC, and e_{h_i} and e_{l_i} are its high and low errors, respectively. The 1-bit DAC errors result from inevitable inaccuracies in the fabrication of the 1-bit DACs and are taken to be arbitrary constants. The multi-bit DAC input, $x[n]$, is a sequence whose range depends on the specific implementation. The digital encoder output is a vector, $\vec{x}[n]$, of N 1-bit sequences, $x_1[n], \ldots, x_N[n]$. The value of each 1-bit sequence is taken to be 1/2 and -1/2 at sample times when it is high and low, respectively. Ideally, a DAC's output is a scaled version of its input. To ensure that the multi-bit DAC approaches this ideal behavior when the 1-bit DAC errors approach zero, the digital encoder determines its output sequences under the following restriction:

$$\sum_{i=1}^{N} (\Delta_i/\Delta_D) \cdot x_i[n] = x[n], \quad (2)$$

where Δ_D is the nominal step size of the multi-bit DAC. Thus, if the 1-bit DAC errors were all zero, (2) implies that the DAC output would be given by

$$y[n] = \Delta_D x[n]. \quad (3)$$

However, the 1-bit DAC errors are not all zero, and, as a result, the multi-bit DAC output is a nonlinear function of the multi-bit DAC input. The error from this nonlinearity can be written as an additive error:

$$y[n] = \Delta_D x[n] + \tilde{e}[n]. \quad (4)$$

The error sequence $\tilde{e}[n]$ often contains a constant offset and scaled version of the input; therefore, it is convenient to write (4) as

$$y[n] = \alpha x[n] + \beta + e[n], \quad (5)$$

where α and β are constants, and $e[n]$ is called the *DAC noise*. In a well-designed system, the DAC noise is a zero-mean sequence that is uncorrelated from the multi-bit DAC input, and the constants α and β depend only on the 1-bit DAC errors.

Mismatch-shaping DACs are designed such that the digital encoder has several possible output vector values, $\vec{x}[n]$, that satisfy (2) for most DAC input values. For example, in a multi-bit DAC in which all the 1-bit DACs have the same nominal step size, a nominal output value of zero is obtained for any output vector with an equal number of high and low bit values. By exploiting this flexibility, the DAC noise is tailored so that its PSD has desired properties regardless of the values of the 1-bit DAC errors. Therefore, a multi-bit DAC is said to *produce DAC noise with a given set of PSD properties* if, for any collection of 1-bit DAC errors, there exist constants α and β, and a sequence $e[n]$ with the given set of PSD properties such that $y[n] = \alpha x[n] + \beta + e[n]$.

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III. THE MISMATCH-SHAPING CONDITION

The theorem below presents a necessary and sufficient condition for the general multi-bit DAC to produce DAC noise with a given set of PSD properties.

Theorem: The multi-bit DAC in Figure 1 produces DAC noise with a given set of PSD properties if and only if there exist $N-1$ sequences $\phi_1[n],\ldots,\phi_{N-1}[n]$ such that:
(a) each digital encoder output is given by

$$x_i[n] = m_i x[n] + \sum_{j=1}^{N-1} d_{i,j}\cdot\phi_j[n], \tag{6}$$

where $d_{i,j}$ and m_i are constants, and
(b) for any selection of the $N-1$ constants $c_1,\ldots,c_{N-1}$, there exist two constants a and b, and a sequence $\varepsilon[n]$ with the given set of PSD properties such that

$$\sum_{j=1}^{N-1} c_j\cdot\phi_j[n] = ax[n]+b+\varepsilon[n]. \tag{7}$$

Proof: Because $x_i[n]$ is interpreted as 1/2 when high and -1/2 when low, (1) can be written as

$$y_i[n] = \xi_i x_i[n] + \gamma_i, \tag{8}$$

where $\xi_i \equiv \Delta_i - (e_{h_i} - e_{l_i})$ and $\gamma_i \equiv (e_{h_i} + e_{l_i})/2$. Given $y[n] = \sum_{i=1}^{N} y_i[n]$, (8) implies that

$$y[n] = \sum_{i=1}^{N} \xi_i x_i[n] + \beta_o, \tag{9}$$

where $\beta_o \equiv \sum_{i=1}^{N}\gamma_i$.

Sufficiency: Assume that the $N-1$ sequences, denoted $\phi_1[n],\ldots,\phi_{N-1}[n]$, exist and satisfy (a) and (b) in the theorem. Substituting (6) into (9) gives

$$y[n] = \underbrace{\left(\sum_{i=1}^{N}\xi_i m_i\right)}_{\equiv\alpha_o} x[n] + \sum_{j=1}^{N-1}\underbrace{\left(\sum_{k=1}^{N}\xi_k d_{k,j}\right)}_{\equiv c_j}\phi_j[n] + \beta_o. \tag{10}$$

Assumption (b) implies that the linear combination of the $N-1$ sequences in (10) can be decomposed as in (7). Thus, given assumption (b), (7) substituted into (10) gives

$$y[n] = \underbrace{(a+\alpha_o)}_{\equiv\alpha} x[n] + \underbrace{b+\beta_o}_{\equiv\beta} + \varepsilon[n], \tag{11}$$

where $\varepsilon[n]$ has the given set of PSD properties. Therefore, the multi-bit DAC produces DAC noise with the given set of PSD properties.

Necessity: To reduce wordiness, all "linear combinations" discussed hereafter are assumed to have constant coefficients. Let $\phi_1[n],\ldots,\phi_N[n]$ be N sequences that result by taking N linearly independent, linear combinations of the digital encoder outputs with $\phi_N[n] = \sum_{i=1}^{N}(\Delta_i/\Delta_D)\,x_i[n]$, which, by (2), implies that $\phi_N[n] = x[n]$. Therefore, if $\vec{x}[n]$ and $\vec{\phi}[n]$ are the N-length column vectors of the digital encoder outputs and the $\phi_j[n]$ sequences, respectively, then there exists an invertible matrix $A \equiv \{a_{j,k}\}_{j,k=1}^{N}$ with $a_{N,k} \equiv \Delta_k/\Delta_D$ such that $\vec{\phi}[n] = A\vec{x}[n]$. This matrix equation implies that, for each j,

$$\phi_j[n] = \sum_{k=1}^{N} a_{j,k}\cdot x_k[n]. \tag{12}$$

Let $D \equiv \{d_{i,j}\}_{i,j=1}^{N}$ be the inverse matrix of A. This implies that $\vec{x}[n] = D\vec{\phi}[n]$ and, for each i,

$$x_i[n] = \sum_{j=1}^{N} d_{i,j}\cdot\phi_j[n]. \tag{13}$$

With $m_i \equiv d_{i,N}$, (13) is identical to (6) because $\phi_N[n] = x[n]$. Therefore, the $N-1$ sequences $\phi_1[n],\ldots,\phi_{N-1}[n]$ satisfy (a) in the theorem.

To show the $N-1$ sequences satisfy (b) in the theorem, assume the multi-bit DAC produces DAC noise with the given set of PSD properties. In (9), ξ_i and β_o are arbitrary constants because each DAC error is an arbitrary constant. Thus, by assumption, *for any* selection of the constants $\xi_1,\ldots,\xi_N$, and β_o, there exist constants a and b, and a sequence $\varepsilon[n]$ with the given set of PSD properties such that

$$\sum_{i=1}^{N}\xi_i x_i[n] + \beta_o = ax[n]+b+\varepsilon[n]. \tag{14}$$

Because the $N-1$ sequences are linear combinations of the digital encoder outputs as given by (12), the linear combination of the $N-1$ sequences in (7) can be written as

$$\sum_{j=1}^{N-1} c_j\cdot\phi_j[n] = \sum_{i=1}^{N}\underbrace{\left(\sum_{j=1}^{N-1} c_j\cdot a_{j,i}\right)}_{\equiv d_i} x_i[n], \tag{15}$$

for any selection of the $N-1$ constants $c_1,\ldots,c_{N-1}$. Since (14) is satisfied for any selection of ξ_i and β_o, suppose $\xi_i = d_i$ for each i, and $\beta_o = 0$. With this selection of $\xi_1,\ldots,\xi_N$, and β_o, the left-hand side of (14) is the same as the right-hand side of (15), which implies (7). Thus, the $N-1$ sequences satisfy (b) in the theorem.

■

IV. ARCHITECTURE ANALYSIS

As an example application of the condition for mismatch shaping, this section analyzes and compares several mismatch-shaping DACs, all of which consist of 1-bit DACs that have the same nominal step size. It is first shown that the DAC noise PSDs are zero at dc in first-order implementations of the vector feedback, DWA, butterfly shuffler, and tree-structured DACs, while the DAC noise in the lowpass P-DWA DAC is not zero at dc. The $N-1$ sequences, $\phi_j[n] = x_{j+1}[n] - x_j[n]$ for $j = 1,\ldots,N-1$, are used to analyze the four first-order DACs as it can be shown that these $N-1$ sequences satisfy (6). It is shown below that the PSD of each of the $N-1$ sequences is zero at dc. This is sufficient to satisfy (7) because, as can be shown, any linear combination of sequences whose PSDs are zero at dc gives rise to a sequence whose PSD is also zero at dc.

An example 5-level (*i.e.*, $N=4$) vector feedback DAC is shown in Figure 2. The digital encoder consists of a *vector quantizer*, a *smallest element* block, two vector adders, and a vector unit delay. The vector $\vec{u}[n]$ consists of N elements, the ith of which is associated with the ith output bit of the digital encoder. At each sample time, n, the vector quantizer determines the $x[n] + N/2$ largest elements of $\vec{u}[n]$, and sets the associated output bits of the digital encoder high and sets the remaining output bits low. The output of the *smallest element* block, $z[n]$, is the minimum value of its vector input. In [1] it is shown that each digital

encoder output can be expressed as $x_i[n] = -z[n] + \varepsilon_i[n]$, where the PSD of $\varepsilon_i[n]$ is zero at dc. Therefore, the PSD of $\phi_j[n] = \varepsilon_{j+1}[n] - \varepsilon_j[n]$ is also zero at dc because it is a linear combination of sequences whose PSDs are zero at dc.

An example 5-level DWA DAC is shown in Figure 3. The digital encoder consists of a thermometer encoder, a barrel shifter and a modulo-N accumlator that consists of an adder, a unit delay, and a modulo-N block. The thermometer encoder selects its bottom $x[n] + N/2$ outputs high and the remaining outputs low. The modulo-N accumulator output, $z[n]$, controls the operation of the barrel shifter as follows: with its inputs and outputs labeled 1 to N from bottom to top, the barrel shifter routes input i to output $1 + (z[n] + i - 1) \bmod N$. For $|x[n]| = N/2$, $\phi_j[n] = 0$ for each j. For $|x[n]| < N/2$, it can be shown that $\phi_j[n] = 1$ if $j = z[n]$, $\phi_j[n] = -1$ if $j = z[n+1]$, and $\phi_j[n] = 0$ otherwise. Therefore, for each j, the nonzero values in $\phi_j[n]$ alternate between 1 and -1, which implies $\left|\sum_{m=0}^{n} \phi_j[m]\right| \leq 1$, for all n. It can be shown that this property implies that the PSD of $\phi_j[n]$ is zero at dc.

An example 5-level butterfly shuffler DAC is shown in Figure 4. The digital encoder consists of a thermometer encoder and *swapper cells*, which are labeled $\hat{S}_{l,m}$. The inputs, $u_0[n]$ and $u_1[n]$, and outputs, $v_0[n]$ and $v_1[n]$, of a swapper cell are 1-bit sequences whose values are taken to be -1/2 at sample times when low and 1/2 at sample times when high. The outputs of the swapper cell are given by

$$v_0[n] = \frac{1}{2}\left(u[n] + \hat{s}[n]\right), \quad \text{and} \quad v_1[n] = \frac{1}{2}\left(u[n] - \hat{s}[n]\right), \tag{16}$$

where $u[n] \equiv u_0[n] + u_1[n]$, and $\hat{s}[n]$ is called the *swapper sequence* whose PSD is zero at dc. Let $\hat{s}_{l,m}[n]$ be the swapper sequence of the swapper cell $\hat{S}_{l,m}$. For the DAC in Figure 4, it can be shown that $\phi_3[n] = \hat{s}_{1,1}[n]$, $\phi_2[n] = \frac{1}{2}\left(\hat{s}_{2,1}[n] + \hat{s}_{2,2}[n] - \hat{s}_{1,1}[n] - \hat{s}_{1,2}[n]\right)$, and $\phi_1[n] = \hat{s}_{1,2}[n]$. For each j in this case and in general, the PSD of $\phi_j[n]$ is zero at dc because it is a linear combination of swapper sequences whose PSDs are zero at dc.

An example 5-level tree-structured DAC is shown in Figure 5. The digital encoder consists of *switching blocks*, which are labeled $S_{k,r}$. If the input to a switching block is denoted $u[n]$, then the two outputs are given by

$$v_0[n] = \frac{1}{2}\left(u[n] + s[n]\right), \quad \text{and} \quad v_1[n] = \frac{1}{2}\left(u[n] - s[n]\right), \tag{17}$$

where $s[n]$ is called the *switching sequence* whose PSD is zero at dc. Let $s_{k,r}[n]$ be the switching sequence for the switching block $S_{k,r}$. For the DAC in Figure 5, it can be shown that $\phi_3[n] = s_{1,1}[n]$, $\phi_1[n] = s_{1,2}[n]$, and $\phi_2[n] = \frac{1}{2}\left(s_{2,1}[n] - s_{1,1}[n] - s_{1,2}[n]\right)$. For each j in this case and in general, the PSD of $\phi_j[n]$ is zero at dc because it is a linear combination of switching sequences whose PSDs are zero at dc.

The P-DWA DAC shown in Figure 6 consists of two 17-level DWA digital encoders and a *divide-by-two* block whose top output is $x[n]/2$ rounded up to the nearest integer, and its bottom output is $x[n]/2$ rounded down to the nearest integer. The motivation behind the design of this architecture is to not only suppress signal-band DAC noise power near dc but to reduce the spurious tones in the DAC noise. Since the difference between the outputs of the divide-by-two block is one when $x[n]$ is odd and zero otherwise, it follows that

$$\sum_{i=17}^{32} x_i[n] - \sum_{j=1}^{16} x_j[n] = x[n] \bmod 2. \tag{18}$$

Since $x[n] \bmod 2$ cannot be written as $\hat{\alpha}x[n] + \hat{\beta} + \hat{e}[n]$, where the PSD of $\hat{e}[n]$ is zero at dc, (7) cannot be satisfied for this PSD property. Therefore, the PSD of the DAC noise is not zero at dc.

Figure 7 displays the output noise PSD from a behavioral simulation of a second-order, analog $\Delta\Sigma$ modulator that employs the P-DWA DAC. The $\Delta\Sigma$ modulator input was a -1dB (relative to full scale) sinusoid with frequency $0.0015 f_s$, where f_s is the sampling frequency. The PSD units are dB relative to Δ^2, where Δ is the ADC step size. The 1-bit DAC errors were chosen as Gaussian random variables with a standard deviation of 1% of the 1-bit DAC's nominal step size. The output noise in the simulation includes the DAC noise and quantization noise. The simulation shows that, as a result of the DAC noise, the noise PSD of the $\Delta\Sigma$ modulator output is not zero at dc. However, the simulation suggests that, compared to conventional DWA, the DAC noise in this implementation has less harmonic distortion, but this spectral property relies on the randomness of the DAC input.

Using the condition for mismatch-shaping, qualitative comparisons can be made concerning the four main DAC architectures. One such comparison can be made regarding how easily each architecture combats harmonic distortion in its DAC noise. The butterfly shuffler and tree-structured DACs generate sequences with the desired spectral properties. If the digital encoder for each DAC ensures that these sequences have bounded PSDs and thus do not contain spurious tones, it can be shown that the resulting DAC noise also does not contain spurious tones. The relative ease for which this is accomplished is shown in [7] where pseudo-random sequences are employed by the switching blocks in both first- and second-order, lowpass tree-structured DACs to eliminate harmonic distortion in the DAC noise. However, the vector feedback and DWA DACs do not generate such sequences, which makes it more difficult to ensure the resulting DAC noise has no spurious tones.

Another comparison can be made concerning the flexibility of each architecture to perform higher-order mismatch shaping. Given $N = 2^b$, where b is a positive integer, the butterfly shuffler DAC generates $b \cdot N/2$ swapper sequences, each of which is required to have the desired PSD properties. Since $b \cdot N/2 > N - 1$ for all $b > 1$, the theorem implies that this digital encoder is generating more sequences than are necessary, all of which are dependent on the DAC input. The dependence on the DAC input makes it difficult to produce swapper sequences and thus DAC noise with higher-order shaping. For example, in a second-order lowpass DAC, it can be shown that each swapper sequence $\hat{s}[n]$ is required to satisfy

$$\left|\sum_{l=0}^{n}\sum_{m=0}^{l} \hat{s}[m]\right| < M,$$

where M is a constant. The more dependence each swapper sequence has on the DAC input, the more difficult it is to keep the magnitude of the double sum bounded. On the other hand, the tree-structured DAC generates $N - 1$ switching sequences with the desired spectral properties, while the vector feedback DAC processes N internal sequences. In comparison to the butterfly shuffler DAC with

$b > 2$, the vector feedback and tree-structured DACs process less internal sequences that have less dependence on the DAC input. This reduced dependence makes it easier to produce DAC noise with higher-order spectral shaping.

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FIGURES

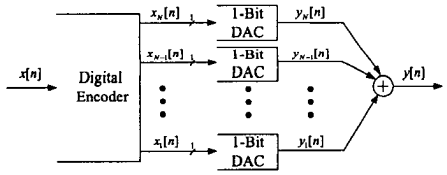

Figure 1: The general multi-bit DAC.

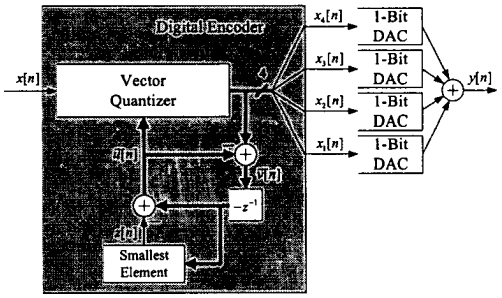

Figure 2: A 5-level vector feedback DAC.

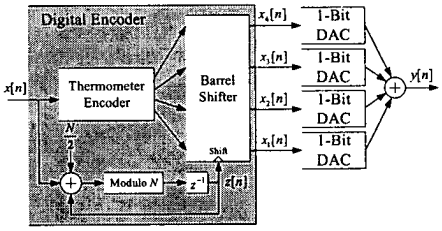

Figure 3: A 5-level DWA DAC.

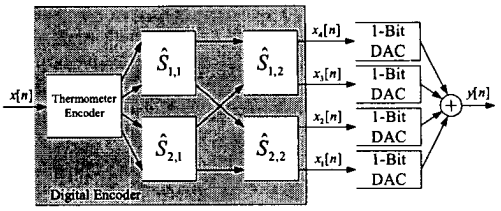

Figure 4: A 5-level butterfly shuffler DAC.

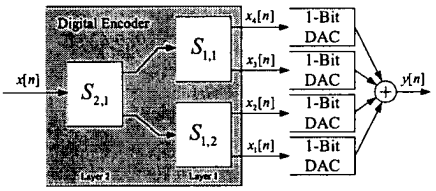

Figure 5: A 5-level tree-structured DAC.

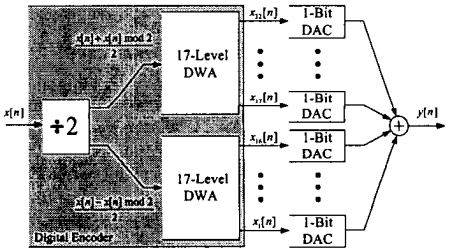

Figure 6: The partitioned DWA DAC.

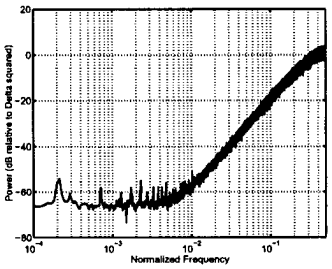

Figure 7: Output noise PSD from a simulation of a second-order $\Delta\Sigma$ modulator using the P-DWA DAC.