Synergistic Design of DSP and Power Amplifiers for Wireless Communications

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***Abstract*—Co-design of digital signal-processing (DSP) algorithms and power-amplifier characteristics can lead to improved efficiency and linearity through a variety of strategies including: predistortion, DSP control over bias conditions, particularly the power supply voltage, and DSP generation of digital input signals for switching amplifiers. This paper discusses several amplifier architectures that exemplify these approaches, including: bias-controlled amplifiers, linear amplification with nonlinear components amplifiers, and class-S amplifiers. We envision for the future a generation of "smart power amplifiers," in which DSP optimization of amplifier parameters is carried out for changing environments.**

***Index Terms*—Delta–sigma modulation, digital radio, RF power amplifier.**

I. Introduction

DIGITAL signal processing (DSP) using Si CMOS integrated circuits is rapidly advancing toward higher throughput and lower power. Fig. 1 illustrates the trend in the power dissipation required to achieve specific processing throughput rates with general-purpose DSP chips. The dramatic power reduction trend is driven by advances in the underlying CMOS technology. With scaled transistor dimensions, higher clock speeds are also attainable. Fig. 2 shows the past and projected clock rate for high-end digital logic chips. In the near future, attainable clock rates will reach into the microwave region. It is likely that an increasing number of the microwave system functions implemented at present in a purely analog fashion may be realized in the future using digital processing. The application of DSP promises significant benefits, among which are the following.

1) The precision attainable with digital techniques is an easily controlled design variable. By changing the word length, one can tailor the dynamic range of the system.
2) The digital circuits are not subject to aging and temperature drift, as are the corresponding analog circuits. Similarly, there is no need for tweaking and tuning of the digital circuits to accommodate manufacturing tolerances.
3) Functions that are linear or nonlinear can be realized, and the degree of nonlinearity can be tightly controlled and reproduced.
4) Testing of circuits can be managed more easily.

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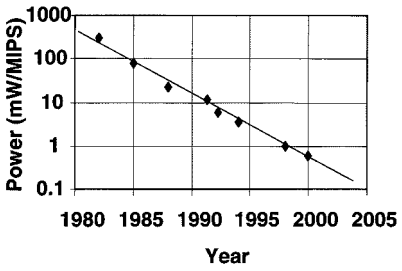


Fig. 1. Trends in power dissipation per unit throughput for commercially available general-purpose digital processing integrated circuits [1].

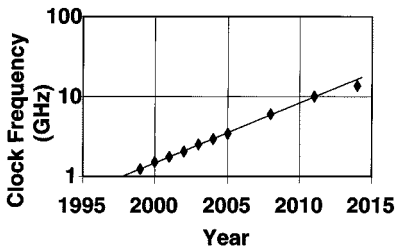


Fig. 2. Trends in clock frequency for high-end application specific CMOS digital integrated circuits (ITRS roadmap, 1999).

5) Digital techniques lead to easier implementation of numerous functions, such as signal storage (or delay).
6) Digital processors can, in principle, be reconfigured to address changing system requirements, leading to systems that are flexible and general purpose. A programmable (software-based) microwave system can, in principle, be implemented.
7) Integrated systems-on-a-chip can be implemented combining microwave and digital functions with the same technology.

The inexorable advance of digital circuits embodied in Moore's Law will permit many of these benefits to be applied in microwave systems. This paper illustrates some approaches to harness DSP in order to improve microwave power amplifiers for wireless communications.

Current development efforts in power amplifiers for mobile communication systems are largely driven by the need to maximize power efficiency (particularly within the handset since the power amplifier is a main determinant of battery talk time). At the same time, with spectrally efficient modulation formats such as QPSK, the amplifier linearity must be sufficiently high that adjacent channel power generation is kept within strict bounds. Compounding these problems is the fact that the output power of a handset typically varies over many orders of magnitude as a result of changing multipath and shadow fading. Fig. 3 shows

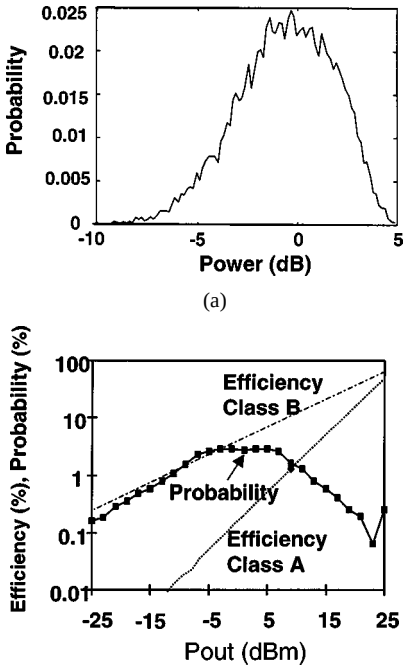


Fig. 3. (a) Output power probability distribution for short (microsecond) time scales. (b) Output power probability distribution for long (millisecond) time scales for representative CDMA transmitters.

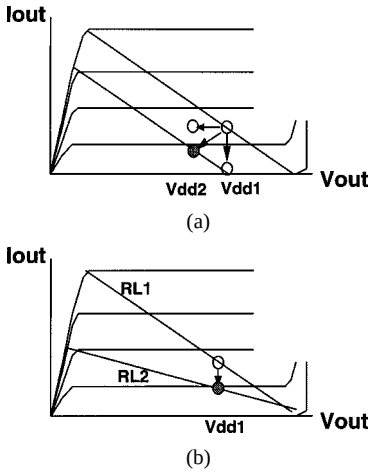


Fig. 4. Amplifier transistor schematic load line analysis showing the desired change in bias point to maintain efficiency as the output power is decreased. (a) With change in bias voltage and current. (b) By change of output load resistance.

a representative output power distribution on a short time scale (resulting from QPSK modulation) and on a longer time scale (as a result of time-varying fading). The average power is much less than the maximum rated amplifier power. In conventional amplifiers, the efficiency decreases dramatically if the output power is backed off from the full rated power. Fig. 3(b) illustrates the falloff of efficiency for ideal class-A and class-B amplifiers at the different power levels used in the handset operation. Most amplifiers in use today are class-AB amplifiers, with efficiency intermediate between these limits. The overall average efficiency $\eta_{\rm ave}$ (which is computed according to $\eta_{\rm ave} = \langle P_{\rm out}\rangle/\langle P_{\rm dc}\rangle$, where $P_{\rm out}$ is the RF output power and $P_{\rm dc}$ is the dc input power) is in the range of only 2%–10%.

There are a number of strategies for the application of DSP to power amplifiers in communications, some of which have already become widespread. Most strategies fall into the following categories.

1) DSP can be used to predistort the RF signals fed into the power amplifiers to improve the overall system linearity. This can, in turn, allow amplifiers to be used closer to compression, where they are more efficient, or it can allow more efficient amplifier architectures to be employed.
2) DSP can be used to control various aspects of the power-amplifier operation (such as bias point), in order to improve its characteristics.
3) DSP can be used to generate signals in new formats that are better suited to the characteristics of efficient amplifiers.

Approach 1), the use of DSP for signal predistortion, is a very significant technique whose usefulness has been amply demonstrated. For base-station power amplifiers, the application of DSP is presently the rule rather than the exception. This technique has been reported extensively in the literature [2]–[7]. Approaches 2) and 3) are less well known, and are highlighted in this paper. Examples are provided of specific amplifier architectures, which implement one or more of the approaches. The bias-controlled amplifier, linear amplification with nonlinear components (LINC) amplifier, and class-S amplifier are discussed in the following sections.

II. Bias-Controlled Amplifier

In class-A power amplifiers, dc-bias conditions are kept constant as the signal input power changes. Since the biases must be set to accommodate the maximum output signal, efficiency perforce suffers with low output power. In most present wireless handset designs, the output bias current is varied in accordance with the signal level over a wide range. This is typically implemented by an analog bias subcircuit or by exploiting the intrinsic characteristics of class-AB amplifiers. Voltage bias variation is an additional dimension, necessary in order to maintain efficiency at peak levels over a range of output powers [6]. Fig. 4(a) illustrates the effect of bias current and voltage variations on the load line for the output transistor. Fig. 4(b) illustrates a related concept, that of variation of the output load resistance, which can result in improved efficiency even with constant bias voltage. Voltage variation can be implemented with a dc–dc converter that transforms battery voltage to a value optimized for the instantaneous output power. We have implemented dc–dc converters with compact size and very rapid response (on the order of the signal envelope for IS-95 CDMA waveforms), which can be used to adjust voltage bias [7]. Fig. 5 illustrates the architecture, in two embodiments. In order to control the bias voltage variation, it is possible to use an analog envelope detector and subsequently add analog circuitry for gain and offset control [see Fig. 5(a)]. The use of DSP [see Fig. 5(b)] provides considerably more flexibility since the relationship between desired power supply voltage and output power can be

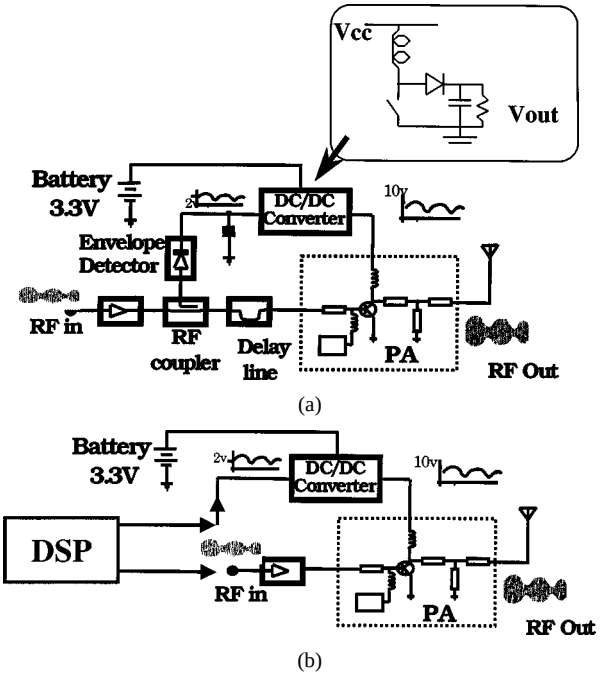


Fig. 5. Architecture of power amplifier with dynamically changing supply voltage. (a) Implementation with analog circuits. (b) Implementation with DSP control.

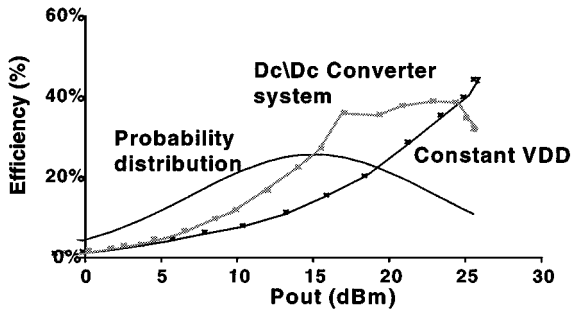


Fig. 6. Experimental measurements of efficiency of amplifier with dynamic supply voltage, and a corresponding amplifier with fixed voltage. Also shown is a schematic output power usage probability distribution.

optimized. At the same time, the dynamic response characteristics of the dc–dc converter can be taken into account (e.g., accommodating the finite response time of the converter). In this configuration, the DSP computes the envelope of the signal, followed by the appropriate control voltage, and computes a suitable delay and pre-emphasis.

The efficiency improvement is illustrated with the data of Fig. 6, which shows the efficiency versus output power measured with the amplifier under fixed power supply voltage, and with the use of the converter to provide variable voltage. Despite the limited efficiency of the converter (80%), the overall system efficiency increases dramatically (by a factor of $\times 1.4$) since the efficiency for relatively low output powers is improved.

Amplifiers with higher efficiency than class A introduce nonlinearities into the output signal, which can lead to objectionable adjacent channel power ratio (ACPR). One approach to reduce this to acceptable levels while retaining an efficiency improvement is with predistortion of the signal fed to the amplifier. Fixed analog predistortion is frequently used. DSP-based

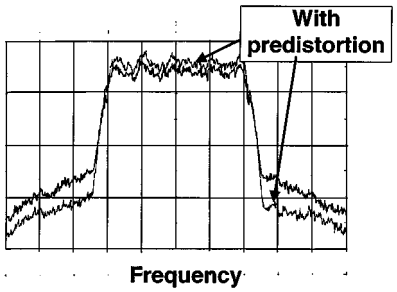


Fig. 7. Measured output spectra for CDMA signal in dynamic supply voltage amplifier with and without predistortion via DSP. Vertical scale: 10 dB/div, horizontal scale: 300 kHz/div, center frequency: 850 MHz.

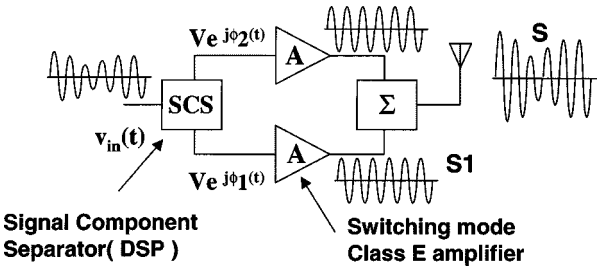
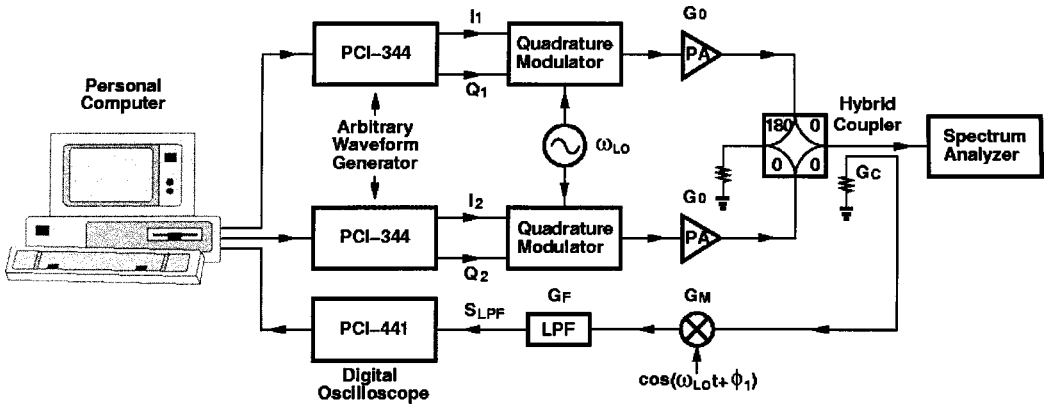


Fig. 8. (a) Schematic architecture of LINC amplifier. (b) Decomposition of signal with time-varying envelope into two components with fixed envelope.

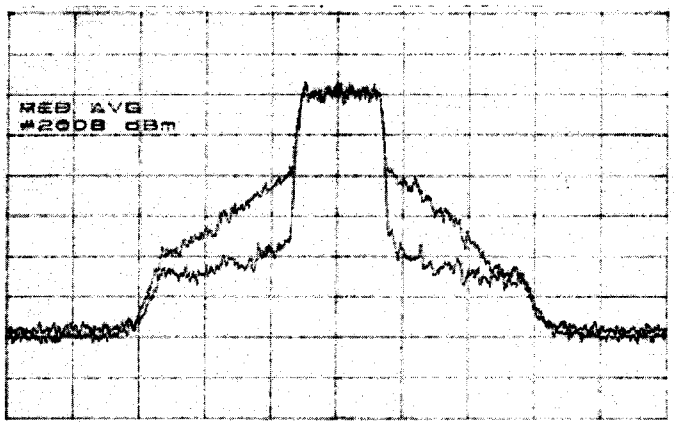
predistortion offers a powerful new set of possibilities since the functions implemented can be flexible and can be made adaptive to accommodate drift in amplifier characteristics [2]–[5]. We implemented DSP-based predistortion in the voltage bias-controlled amplifier since the varying power supply voltage induced changes in gain, which constitutes a source of AM–AM conversion [8]. The DSP used a fixed, rather than adaptive, algorithm in this instance for simplicity since the AM–AM conversion to be compensated has time invariant, and relatively device invariant, characteristics. Fig. 7 illustrates changes in the output spectrum of an IS-95 CDMA signal with and without the use of predistortion in the amplifier. The ACPR was improved by 6 dB in our system with the use of predistortion.

III. LINC Amplifier

In addition to architectures in which DSP is used to control and optimize an analog amplifier, there are other scenarios in which DSP is used to generate fundamentally new signals to drive amplifiers in order to obtain higher efficiency. If the output transistor is used in switching mode, the efficiency can, in principle, be very high since the transistor dissipates little power in its "OFF" state or in its "ON" state. Switching amplifiers, including class-E and class-D amplifiers, have been operated with efficiency of 75% or more, even in the microwave regime [9],



(a)



(b)

Fig. 9. (a) Experimental setup used for elimination of gain and phase errors in a LINC amplifier via DSP. (b) Experimental output spectrum for CDMA signals before and after DSP correction (background technique). Vertical scale: 10 dB/div, horizontal scale: 1 MHz/div, center frequency: 850 MHz.

[10]. Such amplifiers, however, are not capable of reproducing signals with time-varying envelope; the output power level is controlled by the power supply voltage. The switching-mode amplifiers can be used, however, in more complex architectures in order to amplifier general-purpose signals.

One such scenario is the LINC amplifier, illustrated in Fig. 8(a). This concept, also known as the out-phasing amplifier, dates back to the early 1930's [11]–[13]. In modern implementations, DSP is used to form the signal component separator (SCS), which derives from the input signal two separate signals that have constant envelope (but time varying phase) such that when the signals are summed, the appropriate output waveform (with a time-varying envelope) is recovered. The algorithm for generation of the two constant envelope signals, i.e., s_1 and s_2, is illustrated in the phasor diagram of Fig. 8(b). s_1 and s_2 are derived from

$$s_1(t) = s(t) + x_1(t)$$
$$s_2(t) = s(t) - x_1(t)$$

where

$$x_1(t) = ja(t)\sqrt{\frac{a_{\max}^2}{|a^2(t)| - 1}}$$

and $a_{\max}$ is the maximum value of the input signal. $s_1(t)$ and $s_2(t)$ can then be upconverted in the traditional manner. With the resultant constant envelope signals, highly nonlinear amplifiers (such as class-E amplifiers) can be employed. When the signals are recombined, the appropriate envelope variations are recovered as a result of constructive or destructive interference of the component signals. For the practical implementation of this approach, the two amplifiers in the two channels must be very accurately matched regarding amplitude and phase (typically 0.5-dB amplitude matching and 0.3° phase matching). These specifications are extremely difficult to meet in open-loop fashion. We have developed a DSP-based approach to calibrate the system and derive appropriate signal distortions to be introduced into the two channel inputs to maintain high accuracy in the overall output. Fig. 9(a) illustrates the experimental setup used to implement the system. Simple calibration signals are inserted into the amplifier. A receiver is used to sample the output and derive correction factors for the signals in the two paths. A sequence of calibration steps converges rapidly to the desired result. Fig. 9(b) illustrates representative output spectra for CDMA signals before and after the calibration cycle.

IV. Class-S Amplifier

onal approach to employ switching-mode amplifiers for signals with a time-varying envelope is the class-S amplifier,

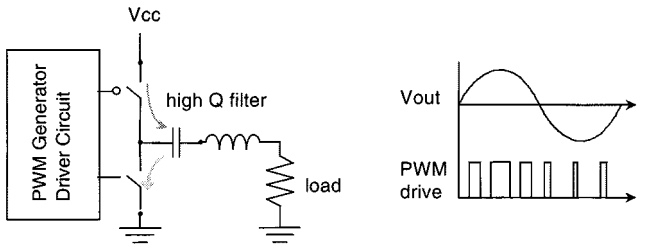


Fig. 10. Schematic structure of class-S amplifier, together with representative output and drive signals.

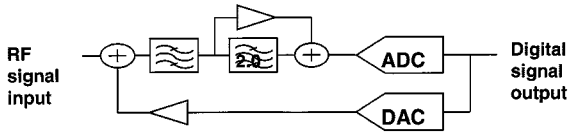
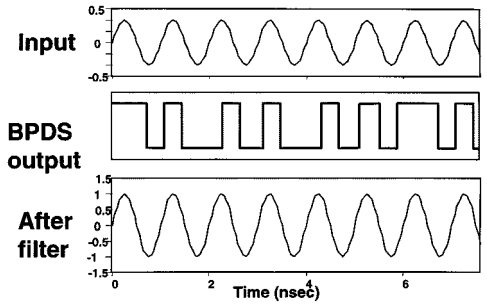


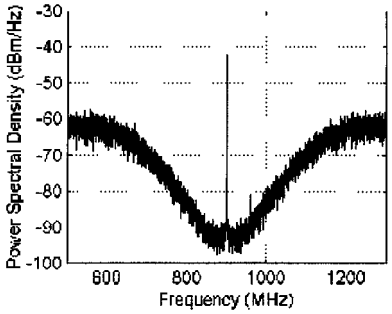
Fig. 11. Representative bandpass delta–sigma modulator.

widely used for audio power amplification. In order to generate waveforms with time-varying envelope (after filtering), pulsewidth modulation can be used, as shown in Fig. 10. A pulse repetition rate substantially ($>10\times$) higher than the desired output center frequency is typically used. The switching mode amplifier can be implemented as a voltage class-D amplifier, schematically shown in Fig. 10, whose output is passed through a series filter that removes the excess quantization noise generated during the modulation process. In fact, the power associated with the undesired out-of-band spectral components is reflected, rather than absorbed in the filter, in a way that preserves high efficiency.

To amplify RF and microwave signals, it is desirable to avoid the need for very high pulse-repetition rates and very tightly controlled pulsewidths. We have investigated amplifiers using the bandpass delta–sigma algorithm to generate digital signal streams that encode analog communication signals of interest. The modulated output consists of a single bit digital data stream (a sequence of pulses of fixed pulse duration). The clock rate can be chosen to be not very much higher than the center frequency of interest (typically $4\times$). The bandwidth of interest, however, must be a relatively small fraction of the center frequency and clock rate, such that a high effective "oversampling ratio" is maintained (where, for this case, the oversampling ratio is the ratio of the clock rate to the signal bandwidth). The unavoidable extraneous signal power present in the digital waveform ("quantization noise") is spectrally shaped to lie out of the signal band of interest, and can be separated with a bandpass filter at the amplifier output. Bandpass delta–sigma modulators can be implemented with analog or digital inputs. Fig. 11 shows the structure of a representative modulator. Fig. 12(a) shows representative waveforms for the input and output in the time domain. A representative spectrum is shown in Fig. 12(b) (corresponding, in this case, to an IS-95 CDMA signal). The spectral shaping of the quantization noise is evident in this figure. In principle, the bandpass delta–sigma signals can be used to drive a switching-mode amplifier with high efficiency [14].



(a)



(b)

Fig. 12. Experimental waveforms and spectra of bandpass delta–sigma signals for CDMA waveforms. The time-domain picture (eye diagram) illustrates the digital nature of the signals. The spectrum shows the desired signal, together with quantization noise shaped out of the band of interest.

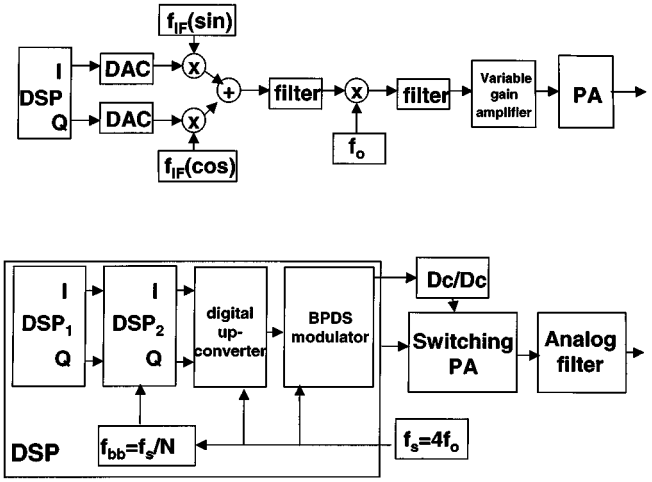


Fig. 13. Comparison of traditional wireless transmitter architecture, based on analog circuits, with a possible DSP-based architecture.

V. Summary and Future Outlook

DSP provides flexibility in the design of waveforms to be used as amplifier analog input signals (by providing controlled amounts of predistortion or by generation of new signal formats, such as in the LINC amplifier). DSP can also be used to control amplifier bias points in accordance with signal levels to optimize performance. In future "smart" power amplifiers, it is likely that numerous amplifier internal variables will be monitored by the DSP, and the information thus derived will be used to reshape the signals and biases. Smart power amplifiers may, for example, sense the chip temperature, or the

status of the output load impedance (which can vary substantially, particularly with handheld units). DSP can also be used to generate digital waveforms to control switching-mode amplifiers. At present, the output of the DSP is at baseband (or IF); conventional mixer techniques are used to upconvert the signals to RF. As the speed of DSP advances, algorithms in which the DSP provides signals at RF can be envisioned (particularly for switching amplifiers, in which the inputs are inherently digital signals). An entirely digital implementation of the entire transmitter chain is shown in Fig. 13. Upconversion to RF and bandpass delta–sigma modulation is accomplished digitally. With a 1-bit digital output, the inaccuracies of high-resolution digital-to-analog converters at high frequency can be circumvented. In the scenario shown, the clock frequency of the DSP is $4\times$ higher than the center frequency of the RF signal. The digital transmitter potentially offers many benefits, including programmability and reconfigurability, absence of tuning or aging problems, as well as easy integrability and testing. It can be an important element in a "soft-ware defined radio" [15].

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Prof. Galton is a member of the IEEE Circuits and Systems Society Board of Governors.