A Dynamic Element Matching Technique for Reduced-Distortion Multibit Quantization in Delta–Sigma ADCs

Eric Fogleman, Member, IEEE, and Ian Galton, Member, IEEE

Abstract—A multibit $\Delta\Sigma$ analog-to-digital converter can achieve high resolution with a lower order modulator and lower oversampling ratio than a single-bit design. However, in a multibit $\Delta\Sigma$ modulator, quantization level errors in the internal multibit quantizer can limit the $\Delta \Sigma$ modulator's signal-to-noise-and-distortion and spurious-free dynamic range. For a CMOS $\Delta\Sigma$ analog-to-digital converter using a flash analog-to-digital converter as its internal quantizer, comparator input offset errors are a significant source of quantization level errors. This paper presents a dynamic element matching (DEM) technique, comparator offset DEM, that modulates the sign of the comparator input offsets with a random sequence and causes the offset errors to appear as white noise and attenuated spurious tones. Measured performance of a prototype $\Delta \Sigma$ modulator IC shows that comparator offset DEM enables it to achieve 98-dB peak signal-to-noise-and-distortion and 105-dB spurious-free dynamic range. Analysis and simulation of comparator offset DEM in a flash analog-to-digital converter with a periodic input and uniform dither give insight into its operation and quantify the spur attenuation it provides.

Index Terms—Analog circuits, analog–digital conversion, CMOS analog integrated circuits, comparators, mixed analog–digital integrated circuits, sigma–delta modulation.

I. INTRODUCTION

T HE DEVELOPMENT of mismatch-shaping multibit digital-to-analog converters (DACs) has helped to make the implementation of high-performance multibit $\Delta\Sigma$ analog-todigital converters (ADCs) feasible. A multibit $\Delta\Sigma$ modulator using a mismatch-shaping feedback DAC can achieve the same signal-to-quantization-noise specifications with a lower order modulator and lower oversampling ratio (OSR) than a single-bit design. The use of multibit feedback also relaxes the slew rate and settling time requirements on the analog integrators. While reducing the $\Delta\Sigma$ modulator order and OSR eases the design of the analog front end, it also reduces attenuation of circuit errors in the quantizer. These errors give rise to spurious tones that can

Manuscript received May 2000; revised January 2001. This work was supported by the National Science Foundation under Grant MIP-9711331. This paper was recommended by Associate Editor G. Cauwenberghs.

E. Fogleman was with the Department of Electrical and Computer Engineering, University of California, San Diego, La Jolla, CA 92093 USA. He is now with Silicon Wave, San Diego, CA 92122 USA (e-mail: fogleman@ieee.org).

I. Galton is with the Department of Electrical and Computer Engineering, University of California, San Diego, La Jolla, CA 92093 USA (e-mail: galton@ece.ucsd.edu).

Publisher Item Identifier S 1057-7130(01)03049-X.

limit the $\Delta \Sigma$ ADCs signal-to-noise-and-distortion (SINAD) and spurious-free dynamic range (SFDR) performance.

In a flash ADC, the most commonly used quantizer in $\Delta\Sigma$ ADCs, quantization level errors stem from the nonideal resistor reference ladder and from comparator input offset errors. Reference ladder errors result from resistor mismatches and scale with the quantization step size. In contrast, CMOS comparator input offsets are dominated by the process' inherent threshold voltage mismatches and become increasingly problematic as the signal swing or the quantization step size are reduced. With the near minimum-size devices required for small-area high-speed comparators, input offsets with standard deviations on the order of 10 mV are typical. Switched-capacitor offset calibration can address this problem, but it significantly increases die area when a large number of comparators are required and large-area metal-metal capacitors are the only available linear capacitor structures.

The technique presented in this paper mitigates the distortion introduced by comparator offsets by modulating the sign of each offset with a random bit sequence. This approach, named *comparator offset DEM* because of its similarity to dynamic element matching (DEM) techniques used in DACs, was developed to address circuit challenges encountered in the design of a high-performance multibit ADC $\Delta\Sigma$ modulator [1]. Because of the choice of architecture and the process limitations, comparator offsets proved to be a barrier to meeting the $\Delta\Sigma$ modulator's 98-dB SINAD and 105-dB SFDR targets. Comparator offset DEM provided a solution to this problem that avoided the use of additional capacitors and enabled the fabricated $\Delta\Sigma$ modulator to meet these aggressive specifications.

The remainder of this paper consists of two main sections and two appendixes. Section II presents the implementation and measured performance of comparator offset DEM in the prototype $\Delta\Sigma$ ADC. Section III presents the signal-processing details of the technique. Appendixes A and B give a detailed derivation of the theoretical results presented in Section III.

II. IMPLEMENTATION IN ADC $\Delta\Sigma$ Modulator

The $\Delta\Sigma$ modulator mentioned above is a second-order design operating at 3.072 MHz with an OSR of 64. The prototype was fabricated in a 3.3-V 0.5- μ m single-poly triple-metal CMOS process, and it achieves 98-dB peak SINAD and 105-dB SFDR [1]. As shown in Fig. 1, it uses two delaying switched-capacitor integrators, a 33-level mismatch-shaping DAC, and a



Fig. 1. $\Delta\Sigma$ modulator circuit topology.



Fig. 2. Flash ADC circuit topology.

33-level quantizer [2], [3]. The differential input quantizer was realized using a pair of single-ended 33-level flash ADCs and digital subtraction of the outputs to reject common-mode noise. Noise-shaped requantization was used to reduce the 65-level difference signal to 33-levels for use in the mismatch-shaping DAC encoder [4].

The topology of a single-ended 33-level flash ADC is shown in Fig. 2. It consists of a unit resistor ladder to set the quantization levels and a bank of 1-bit ADCs to compare the input signal to each quantization level. A standard clocked comparator is used to implement each of the 1-bit ADCs. Each comparator's output is equal to one if the input exceeds its reference level, and is zero otherwise. The 32 comparator outputs form a thermometer-coded representation of the quantized signal. The thermometer to binary decoder in Fig. 2 is a device that generates a binary representation equal to the number of nonzero 1-bit ADC outputs. As mentioned in the introduction, the major sources of error in the flash ADC are resistor mismatches in the unit resistor ladder and input offset errors in the comparators.

In the prototype, the expected level of device matching and the limited signal swing implied that comparator input offsets were the dominant error source. The input range of the flash ADCs was set by the integrators' 1.5 V \pm 0.5 V single-ended output swing. For 33-level quantization, the ADCs' nominal step size Δ was 31.25 mV and their reference levels ref_k, k = 1, ..., 32, ranged from 1.0 V + $\Delta/2$ to 2.0 V - $\Delta/2$. Given Gaussian-distributed offsets with a standard deviation of 10 mV, a large percentage of the comparators would be likely to have input offsets comparable to Δ in magnitude. In contrast, Gaussian-distributed resistor mismatches with a standard deviation of 1% of the unit resistance value would yield reference level errors with standard deviations below 0.9 mV. Behavioral simulations of the $\Delta\Sigma$ modulator with the expected level of comparator offsets indicated that the attenuation provided by the noise transfer function was not sufficient to guarantee meeting the 105-dB SFDR target.

Comparator offset DEM is implemented in the flash ADC using the swapper cells S_1 and S_2 at the analog input and digital output of each comparator, as shown in Fig. 3. The control signal r[n] is a 1-bit, ± 1 pseudorandom sequence. When r[n] = 1, the direct paths through S_1 and S_2 are chosen, and

$$y_k[n] = \begin{cases} 1, & v_{in}[n] > ref_k + V_{osl} \\ 0, & otherwise. \end{cases}$$

When r[n] = -1, the swapped paths through S_1 and S_2 are chosen, and

$$y_k[n] = \begin{cases} 1, & v_{\rm in}[n] > {\rm ref}_k - V_{\rm osk} \\ 0, & \text{otherwise.} \end{cases}$$

Thus, the swapping shown in Fig. 3 gives rise to two quantization thresholds per comparator selected by the value of the pseudorandom sequence r[n].

The comparator offset DEM circuitry was added to the $\Delta\Sigma$ modulator with minimal increase in die size. Each swapper cell was implemented using four minimum-size transmission gates. The 1-bit pseudorandom sequence was provided by the $\Delta\Sigma$ modulator's existing sequence generator and required no additional area. The comparator offset DEM hardware occupied only 1.5% of the total chip area and required 65% less area per comparator than the switched-capacitor offset calibration approach considered for the design [5].



Fig. 3. Flash ADC with comparator offset DEM.

 TABLE I

 MEASURED SFDR PERFORMANCE FOR FULL-SCALE TWO-TONE INPUT SIGNAL

Device	SFDR (dB) DEM off	SFDR (dB) DEM on	Improvement (dB)
1	104.7	108.4	3.7
2	108.2	108.3	0.1
3	104.6	108.4	3.8
4	99.3	108.4	9.1
5	106.6	108.6	2.0
6	107.4	108.2	0.8

Measured results show that comparator offset DEM provides a significant reduction of spurious tones in the $\Delta\Sigma$ modulator output. The $\Delta\Sigma$ modulator was tested with a variety of single-tone and two-tone inputs, and performance with and without DEM was compared by enabling and disabling the random bit. Because the errors due to comparator offsets are attenuated by the quantization noise transfer function, the most dramatic improvement in in-band SFDR occurred for two-tone inputs generating spurious components near the 24-kHz passband edge. Table I summarizes measured SFDR performance for six randomly chosen prototype $\Delta\Sigma$ modulators. For this test, the input is a full-scale two-tone signal with components at 500 Hz and 21 kHz. Without comparator offset DEM, the measured SFDR ranged from 99.3 to 108.2 dB. Comparator offset DEM improved the SFDR to over 108 dB for all six devices. Fig. 4 shows the output power spectral density (PSD) for device 4. For this device, comparator offset DEM provided over 15-dB attenuation of the second-order intermodulation products at 20.5 and 21.5 kHz.

III. COMPARATOR OFFSET DEM SIGNAL-PROCESSING DETAILS

Unlike DAC dynamic element matching techniques that fully whiten mismatch errors for arbitrary input signals, comparator offset DEM requires an input with a random component to achieve a significant reduction in spurious tones. This random component is necessary to make both thresholds' modulated values affect the output with nearly equal probability. When the flash ADC is used within a multibit $\Delta\Sigma$ modulator having a small amount of input-referred noise, the quantization noise present at the flash ADC's input provides this randomness [6].

To characterize the performance of comparator offset DEM, the (L + 1)-level flash ADC of Fig. 3 is analyzed with a deterministic input x[n] plus independent, identically distributed (i.i.d.) dither w[n]. By appropriate choice of the dither's probability density function—e.g., uniform over $(-\Delta/2, \Delta/2)$ or triangular over $(-\Delta, \Delta)$ —the error due to ideal quantization appears as white noise at the flash ADC's output [7], [8]. As a result, spurious tones at the flash ADC output are due only to misplaced quantization thresholds.

The flash ADC is first analyzed with comparator offset DEM disabled—i.e., r[n] = 1 for all *n*—then with DEM enabled to show the performance improvement relative to a conventional implementation. It is shown that comparator offset DEM causes the offset errors to appear as white noise and attenuated spurious components, and that under certain conditions, it completely eliminates spurious tones.

A. Nonideal Flash ADC Model

For analysis, the flash ADC shown in Fig. 3 is modeled as a memoryless transfer function $g_y(v_{in}, r)$, where v_{in} is the instantaneous value of the flash ADC input and r is the instantaneous value of the ± 1 random control bit. The flash ADC output sequence y[n] is then

$$y[n] = g_y(v_{\rm in}[n], r[n])$$

where $v_{in}[n]$ denotes the flash ADC input sequence and r[n] denotes the ± 1 random control bit sequence.

The ideal resistor ladder shown in Fig. 3 is driven with reference voltages $+V_{\text{ref}}$ and $-V_{\text{ref}}$, and the ladder provides quantization thresholds $\operatorname{ref}_k = k\Delta - ((L+1)/2)\Delta$, $k = 1, 2, \ldots L$, with a quantization step size $\Delta = (2V_{\text{ref}}/L)$. Let V_{osk} , k = $1, 2, \ldots L$, denote the static input offsets of the comparators within the 1-bit ADCs. By defining the unit step function u(x)as

$$u(x) = \begin{cases} 1, & x > 0\\ 0, & \text{otherwise} \end{cases}$$

the transfer function of the kth 1-bit ADC can be expressed as

$$g_{y_k}(v_{\text{in}}, r) = u(v_{\text{in}} - \text{ref}_k - r \cdot V_{\text{osk}}).$$
(1)

The transfer function $g_y(v_{in}, r)$ is formed by summing the L comparator outputs and adding offset of -L/2

$$g_y(v_{\rm in}, r) = -\frac{L}{2} + \sum_{k=1}^{L} u(v_{\rm in} - \operatorname{ref}_k - r \cdot V_{\rm osk}).$$
 (2)



Fig. 4. Measured $\Delta\Sigma$ modulator results. (a) DEM disabled and (b) DEM enabled.

The L/2 offset is added in (2) so $g_y(v_{in}, r)$ will range from -L/2 to L/2 rather than from zero to L.

In the absence of comparator offsets, (2) is the transfer function of an ideal uniform quantizer. Fig. 5(a) shows $g_y(v_{\rm in}, r)$ near ref_k for $r = \pm 1$. The dotted-line graph in Fig. 5(a) shows the ideal flash ADC transfer function for $V_{\rm osk} = 0$.

The flash ADC transfer function can be viewed as a linear function plus an error function. Let $\alpha_q = 1/\Delta$ denote the quantizer's effective gain, let $g_{e_q}(v_{\rm in})$ denote the transfer function for error due to ideal quantization, and let $g_{e_{\rm os}}(v_{\rm in}, r)$ denote the transfer function for error due to comparator offsets. Thus

$$g_y(v_{\rm in}, r) = \alpha_q v_{\rm in} + g_{e_q}(v_{\rm in}) + g_{e_{\rm os}}(v_{\rm in}, r)$$
 (3)

where

$$g_{e_q}(v_{\rm in}) = -\alpha_q v_{\rm in} - \frac{L}{2} + \sum_{k=1}^N u(v_{\rm in} - {\rm ref}_k), \quad (4)$$

$$g_{e_{\rm os}}(v_{\rm in}, r) = \sum_{k=1}^{N} u(v_{\rm in} - \operatorname{ref}_k - r \cdot V_{\rm osk}) - u(v_{\rm in} - \operatorname{ref}_k).$$
(5)

Fig. 5(b) shows the total error transfer function $g_{e_q}(v_{in}) + g_{e_{os}}(v_{in}, r)$ for $r = \pm 1$, with $g_{e_q}(v_{in})$ shown as a dashed-line graph. The comparator offset error transfer function $g_{e_{os}}(v_{in}, r)$ is shown in Fig. 5(c). It consists of rectangular pulses near each ref_k and is nonzero in the regions where the flash ADC's output differs from that of an ideal quantizer.

Let the flash ADC input sequence be $v_{in}[n] = x[n] + w[n]$, where x[n] is a deterministic input sequence and w[n] is an i.i.d. dither sequence. As above, x and w denote the instantaneous values of the input and dither. Let the characteristic function of w, $\Phi_w(u)$, satisfy

$$\Phi_w\left(\frac{2\pi l}{\Delta}\right) = \begin{cases} 1, & l = 0\\ 0, & l = \pm 1, \pm 2, \dots \end{cases}$$
(6)



where

$$\Phi_w(u) = \int_{-\infty}^{\infty} f_w(w) e^{juw} \, dw.$$

Provided that $|v_{in}| < V_{ref}$, the use of i.i.d. dither satisfying (6)—e.g., uniform dither on $(-\Delta/2, \Delta/2)$ or triangular dither on $(-\Delta, \Delta)$ —implies that $e_q[n]$ is an i.i.d. sequence of random variables independent of x[n] and uniformly distributed on $(-\Delta/2, \Delta/2)$ [7], [8].

It follows from (3) that the flash ADC output sequence is

$$y[n] = \alpha_q x[n] + \alpha_q w[n] + e_q[n] + e_{\rm os}[n]$$

where $e_q[n] = g_{e_q}(x[n] + w[n])$ and $e_{os}[n] = g_{e_{os}}(x[n] + w[n], r[n])$. It is shown in Appendix B, Claim B13, that the time average PSD of the flash ADC output is given by

$$S_{yy}(e^{j\omega}) = \alpha_q^2 S_{xx}(e^{j\omega}) + \overline{\sigma}^2 + \overline{\mu}\,\delta[m] + S'(e^{j\omega}) \quad (7)$$

where $S_{xx}(e^{j\omega})$ is the time average PSD of the input $x[n], \overline{\sigma}^2$ is a white noise term, $\overline{\mu} \delta[m]$ is a dc offset term, and

$$S'(e^{j\omega}) = \sum_{m=-\infty}^{\infty} \overline{R}'[m] e^{-j\omega m}$$
(8)

where

$$\overline{R}'[m] = \lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} \alpha_q x[n] \mathbb{E} \{ e_{\text{os}}[n+m] \} + \alpha_q x[n+m] \mathbb{E} \{ e_{\text{os}}[n] \} + R_{e_{\text{os}}e_{\text{os}}}[n,m].$$
(9)

In (9), E{·} is the statistical expected value and $R_{e_{os}e_{os}}[n, m] = E\{e_{os}[n]e_{os}[n+m]\}$ is the statistical autocorrelation of $e_{os}[n]$. Thus, $S'(e^{j\omega})$ represents noise and spurious tones resulting from comparator offsets.

To evaluate (9), an expression for $E\{e_{os}[n]\}$ is required, where the expectation is taken over the random dither w[n]and the random sequence r[n]. Because w[n] is independent of r[n], the expectation can be expressed as

$$E\{e_{os}[n]\} = E_w \{E_r\{g_{e_{os}}(x[n] + w, r)\}\}$$
(10)









Fig. 5. Flash ADC behavior at ref_k for $r = \pm 1$: (a) quantizer transfer function $(g_y(V_{in}, r); (b) \text{ total quantization error } g_e(v_{in}, r) \text{ (ideal shown with dashed line); and (c) error due to comparator offsets <math>g_{eos}(v_{in}, r)$.

where indexes have been dropped on w and r because they are each i.i.d. random sequences.

Let the average offset error as a function of the deterministic input x[n] be denoted by

$$\overline{g}_{e_{\rm os}}(x) = \mathcal{E}_w \left\{ \mathcal{E}_r \left\{ g_{e_{\rm os}}(x+w, r) \right\} \right\}. \tag{11}$$

Thus, $E\{e_{os}[n]\} = \overline{g}_{e_{os}}(x[n])$. Evaluating the expectation over w in (11) gives

$$\overline{g}_{e_{\rm os}}(x) = \int_{-\infty}^{\infty} \operatorname{E}_r \left\{ g_{e_{\rm os}}(v, r) \right\} f_w(v - x) \, dv. \tag{12}$$

Because (12) is in the form of a convolution integral, the transfer function $\overline{g}_{e_{os}}(x)$ can be computed graphically by evaluating $E_r\{g_{e_{os}}(v, r)\} * f_w(-v)$.

B. Conventional Flash ADC

Comparator offset DEM is disabled by setting r[n] = 1for all n. For illustration purposes, w[n] is assumed to be uniform dither on $(-\Delta/2, \Delta/2)$. The error function $g_e(v_{\rm in}) = g_{e_{\rm os}}(v_{\rm in}) + g_{e_q}(v_{\rm in})$ and comparator offset error component $g_{e_{\rm os}}(v_{\rm in}) + g_{e_q}(v_{\rm in})$ and comparator offset error component $g_{e_{\rm os}}(v_{\rm in})$ are shown in Fig. 6(a) and (b), respectively. The shifted dither probability density function $f_w(v_{\rm in} - x)$ is also shown in Fig. 6(b). Because r[n] = 1 for all n, $E_r\{e_{\rm os}(v_{\rm in}, r)\} = g_{e_{\rm os}}(v_{\rm in}, 1)$. The transfer function $\overline{g}_{e_{\rm os}}(x)$, shown in Fig. 6(c), has been computed graphically by evaluating $g_{e_{\rm os}}(v, 1) * f_w(-v)$.

As shown in Fig. 6(c), for $|V_{\text{osi}}| \neq |V_{\text{osj}}| \neq 0$, $\overline{g}_{e_{\text{os}}}(x)$ is nonzero for all x except the points where it changes sign. Thus, for almost all signals of interest, the sequence $\mathbb{E}\{e_{\text{os}}[n]\}$ is nonzero, and $S'(e^{j\omega})$ contributes spurious tones to $S_{yy}(e^{j\omega})$.



Fig. 6. Flash ADC error transfer functions without comparator offset DEM: (a) $g_e(V_{in})$, (b) $g_{e_{os}}(v_{in})$, and (c) $\overline{g}_{e_{os}}(x)$.



Fig. 7. Flash ADC error transfer functions with comparator offset DEM: (a) $g_e(v_{in})$, (b) $g_{e_{OS}}(v_{in}, r)$, (c) $E_r\{g_{e_{OS}}(v_{in}, r)\}$, and (d) $\overline{g}_{e_{OS}}(x)$.

For example, consider an input x[n] with period N. The periodicity of x[n] implies that $\mathbb{E}\{e_{os}[n+m]\}$ would be periodic in mwith period N. Therefore, $\overline{R}'[m]$ would also be periodic in mwith period N, and its Fourier transform $S'(e^{j\omega})$ would consist exclusively of spurious tones.

C. Flash ADC with Comparator Offset DEM

Comparator offset DEM is enabled by letting r[n] be an i.i.d. random sequence independent of w[n] with $P\{r = 1\} = P\{r = -1\} = 1/2$. Thus, the polarity of the comparator offsets is modulated as given by (1). As in



Fig. 8. Simulation results for five-level flash ADC with x[n] in $\overline{g}_{e_{OS}}(x) = 0$ regions: (a) DEM off and (b) DEM on.



Fig. 9. Simulation results for five-level flash ADC with x[n] in $\overline{g}_{e_{05}}(x) \neq 0$ regions: (a) DEM off and (b) DEM on.

the previous case, w[n] is assumed to be uniform dither on $(-\Delta/2, \Delta/2)$.

The error transfer functions $g_e(v_{in})$ and $g_{e_{os}}(v_{in}, r)$ for $r = \pm 1$ are shown in Fig. 7(a) and (b), respectively. The shifted dither probability density function $f_w(v_{in} - x)$ is also shown in Fig. 7(b). The transfer function $E_r\{g_{e_{os}}(v_{in}, r)\}$, shown in Fig. 7(c), is obtained by averaging over the two states of r.

From $\overline{g}_{e_{os}}(x)$, shown in Fig. 7(d), it can be seen that the key benefit provided by comparator offset DEM is the creation of large zero regions in the $\overline{g}_{e_{os}}(x)$ transfer function by producing equal-area positive and negative error regions in e_{os} centered at each threshold. When $f_w(-v)$ is convolved with $E_r\{g_{e_{os}}(v, r)\}$, as shown in Fig. 7(c), the positive and negative errors cancel each other for much of the flash ADC's input range. The regions where $\overline{g}_{e_{os}}(x) = 0$ correspond to those input values where the dither pdf covers both the positive and negative error regions, giving equal probability of positive and negative comparator offset error. The nonzero regions centered between the quantizer thresholds correspond to input values where the dither pdf does not cover both error regions equally and the probabilities of positive and negative errors are unequal.

An input x[n] that completely avoids the nonzero regions of the transfer function $\overline{g}_{e_{os}}(x)$ has $E\{e_{os}[n]\} = 0$ for all n. As shown in Appendix B, Claim B8, $e_{os}[n]$ is a sequence of independent random variables for any deterministic input x[n]. Thus

$$R_{e_{\rm os}e_{\rm os}}[n, m] = \delta[m] \mathbf{E}\{e_{\rm os}[n]^2\}.$$

Using this result in (9), it follows that

$$\overline{R}'[m] = \lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} \delta[m] \mathbb{E} \left\{ e_{\text{os}}[n]^2 \right\} = \delta[m] \overline{R}'[0].$$

Thus, (7) implies

$$S_{yy}(e^{j\omega}) = \alpha_q^2 S_{xx}(e^{j\omega}) + \overline{\sigma}^2 + (\overline{\mu} + \overline{R}'[0]) \,\delta[m].$$

Therefore, $S_{yy}(e^{j\omega})$ consists only of a scaled version of the deterministic input signal, a dc component, and white noise. Because $\overline{\sigma}^2$ depends on $e_{cs}[n]$, the power of the offset errors is still present in y[n], but comparator offset DEM causes it to appear entirely as white noise.

For an input with some samples in the nonzero regions of $\overline{g}_{e_{os}}(x)$, the offset errors give rise to both white noise and attenuated spurious components in $S_{yy}(e^{j\omega})$. The attenuation of the spurious tones results from the reduction in magnitude of $E\{e_{os}[n]\}$ provided by comparator offset DEM. Simulation results for a wide range of inputs indicate that significant spur attenuation can be achieved in this case.

For input signals falling in the nonzero regions of $\overline{g}_{e_{os}}(x)$ on every sample, there exist offset distributions such that comparator offset DEM provides little reduction of the peak spurious component. However, signals of this type are unlikely to occur in an oversampled converter.

D. Simulation Example

To illustrate the partial and full spur attenuation predicted by the analysis, Figs. 8 and 9 show simulation results for a fivelevel flash ADC with random errors $|V_{osk}| < \Delta/8$ and uniform i.i.d. dither w[n]. In Fig. 8, the input signal was chosen to be $x[n] = \Delta \sin((\pi/4)n) + (\Delta/8)$. Since the offset errors are bounded by $\Delta/8$, this choice of input forces every sample to land in a region where $\overline{g}_{e_{os}}(x) = 0$, resulting in $E\{e_{os}[n]\} = 0$. The PSD in Fig. 9(b) shows that with DEM enabled, no spurs are visible in the output, and supports the theoretical result that comparator offset errors are completely whitened.

The results for the same flash ADC with an input $x[n] = \Delta \sin((\pi/4)n)$ are shown in Fig. 9. This choice of input forces half of its samples to land in the mid-threshold regions where $\overline{g}_{e_{os}}(x) \neq 0$. Without comparator offset DEM, as shown in Fig. 8(a), the flash ADC has an SFDR of 24.4 dB. With DEM enabled as shown in Fig. 8(b), the third harmonic is reduced significantly, but the SFDR is limited to 26.5 dB by the second harmonic. As predicted, the DEM attenuates the spurious tones but does not completely eliminate them.

IV. CONCLUSION

A comparator offset DEM technique for mitigating the distortion caused by comparator offsets in the flash ADC of a multibit ADC $\Delta\Sigma$ modulator has been presented. Comparator offset DEM was implemented to solve circuit challenges encountered in developing a high-performance $\Delta\Sigma$ modulator IC prototype. The DEM technique provided a significant reduction of offset-related spurious tones and enabled the $\Delta\Sigma$ modulator to meet its aggressive SINAD and SFDR targets.

Analysis of comparator offset DEM for deterministic inputs with i.i.d. dither shows the mechanism by which it attenuates offset-related spurs and describes the conditions under which offset-related spurs are completely whitened. The combination of a random component on the flash ADC's input and random DEM switching creates regions on the quantizer's transfer characteristic where positive and negative quantizer errors occur with equal probability, causing the static offset errors to appear as white noise rather than spurious tones. Though the analysis was developed in the context of comparator offsets, the result can be applied without modification to any scheme where two nonideal quantization thresholds are symmetrically modulated around the ideal quantization threshold.

APPENDIX A

This Appendix presents definitions and theorems used in Appendix B to derive the main theoretical results of this paper. Let the *statistical mean* of a sequence z[n] be defined as

$$\mu_{z}[n] = \mathbf{E}\left\{z[n]\right\}$$

where $E\{\cdot\}$ denotes the statistical expectation operator. Let the *time average* of z[n] be defined as

$$\overline{M}_z = \lim_{P \to \infty} \frac{1}{P} \sum_{n=0}^{P-1} z[n].$$

Let the *statistical autocorrelation* of z[n] be defined as

$$R_{zz}[n, m] = \operatorname{E}\left\{z[n]z[n+m]\right\}$$
(13)

and let the *time average autocorrelation* of z[n] be defined as

$$\overline{R}_{zz}[m] = \lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} z[n]z[n+m].$$
(14)

Similarly, let the *statistical cross-correlation* of v[n] and z[n] be defined as

$$R_{vz}[n, m] = \mathbb{E}\left\{v[n]z[n+m]\right\}$$
(15)

and let the *time average cross-correlation* of v[n] and z[n] be defined as

$$\overline{R}_{vz}[m] = \lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} v[n]z[n+m].$$
(16)

The *time average power spectral density*, referred to here as the PSD, is defined as the Fourier transform of (14)

$$S_{zz}(e^{j\omega}) = \sum_{m=-\infty}^{\infty} \overline{R}_{zz}[m]e^{-j\omega m}.$$
 (17)

Theorem A1: Suppose that w[n] and r[n] are sequences of independent random variables. If $g_n(w, r)$ is a sequence of memoryless, deterministic functions, then $z[n] = g_n(w[n], r[n])$ is a sequence of independent random variables.

Proof: Fix a positive integer K, and for k = 1, ..., K, choose real numbers z_k and integer indexes n_k , where $n_i \neq n_j$ for $i \neq j$. Let

$$A_{k} = \{((w, r): g_{n_{k}}(w, r) \le z_{k}\}$$

for k = 1, ..., K. Because w[n] and r[n] are independent random sequences, the events

$$\{z[n_k] \le z_k\} = \{(w[n_k], r[n_k]) \in A_k\}$$

are independent for $k = 1, \ldots, K$. Therefore

$$P\{z[n_1] \le z_1, \dots, z[n_K] \le z_K\} = P\{z[n_1] \le z_1\} \dots P\{z[n_K] \le z_K\}.$$

Theorem A2: Suppose w[n] and r[n] are sequences of independent random variables. If $g_n(w, r)$ and $h_n(w, r)$ are sequences of memoryless, deterministic functions, then the random variables $z[n] = g_n(w[n], r[n])$ and $v[n+m] = h_n(w[n+m], r[n+m])$ are independent for all integers n and for all integers $m \neq 0$.

Proof: Fix an integer n, a nonzero integer m, and real numbers z and v. Let

$$A = \{(w, r): g_n(w, r) \le z\}$$

and

$$B = \{(w, r): h_{n+m}(w, r) \le v\}.$$

Because w[n] and r[n] are independent random sequences, the events

$$\begin{aligned} &\{z[n] \leq z\} = \{(w[n], r[n]) \in A\} \\ &\{v[n+m] \leq v\} = \{(w[n+m], r[n+m] \in B\} \end{aligned}$$

are independent. Therefore

$$\begin{split} P\left\{ z[n] \leq z, \, v[n+m] \leq v \right\} \\ &= P\left\{ z[n] \leq z \right\} P\left\{ v[n+m] \leq v \right\}. \end{split}$$

Theorem A3: Given z[n], a sequence of independent random variables, suppose there exists a positive real number A such that $P\{|z[n]| < A\} = 1$ for all n. If \overline{M}_z exists, then

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} \operatorname{E} \left\{ z[n] \right\} = \overline{M}_{z}$$

with probability 1.

Proof: Note that for all n

$$0 \le \operatorname{Var}(z[n]) \le \operatorname{E}\{z[n]^2\} \le \operatorname{E}\{A^2\} = A^2.$$

Thus

$$0 \le \sum_{n=1}^{\infty} \frac{\operatorname{Var}(z[n])}{n^2} < A^2 \sum_{n=1}^{\infty} \frac{1}{n^2} < \infty.$$
(18)

Given that z[n] is independent, the Kolmogorov criterion states that (18) is sufficient for z[n] to obey the Strong law of large numbers [9]

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} (z[n] - \mathbf{E}\{z[n]\}) = 0$$

with probability 1. Because \overline{M}_z exists

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} \mathrm{E} \{ z[n] \} = \overline{M}_z$$

with probability 1.

Lemma A: If z[n] is a sequence of independent random variables, then for all integers m and for p = 0, 1, ..., |m|

$$r_p[n] = z [n (|m|+1) - p] z [n (|m|+1) - p + m]$$

is a sequence of independent random variables.

Proof: First consider m = 0. Because z[n] is independent, $r_0[n] = z[n]^2$ is independent by Theorem A1. [Let $g_n(z, r) = z^2$].

Now consider $m \neq 0$. Fix $p \in \{0, 1, ..., |m|\}$. Fix a positive integer K, and for k = 1, ..., K, choose real numbers ρ_k

and integers n_k , where $n_i \neq n_j$ for $i \neq j$. To show that the events

$$\{ r_p[n_k] \le \rho_k \}$$

= $\{ z [n_k (|m|+1) - p] z [n_k (|m|+1) - p + m] \le \rho_k \}$

are independent for k = 1, ..., K, it is sufficient to show that the indexes are unique.

For m = 0, $n_i \neq n_j$ immediately implies $n_i(|m|+1) - p \neq n_j(|m|+1) - p$.

Now consider $m \neq 0$. Suppose for the sake of contradiction that $n_i(|m|+1) - p = n_j(|m|+1) - p + m$. This would imply

$$n_i = n_j + \frac{m}{|m|+1}.$$

This is a contradiction because n_i and n_j are integers and $m \neq 0$. Therefore, the independence of z[n] and the uniqueness of the indexes imply

$$P\{r_p[n_1] \le \rho_1, \dots, r_p[n_K] \le \rho_K\} = P\{r_p[n_1]\} \dots P\{r_p[n_K]\}.$$

Theorem A4: Given z[n], a sequence of independent random variables, suppose there exists a positive real number A such that $P\{|z[n]| < A\} = 1$ for all n. If $\overline{R}_{zz}[m]$ exists, then

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} R_{zz}[n, m] = \overline{R}_{zz}[m]$$

with probability 1.

Proof: To prove the result, the sequence z[n]z[n + m] is decomposed into a finite collection of infinite, independent random sequences that satisfy the Kolmogorov criterion and therefore obey the Strong law of large numbers. Summing over the finite collection completes the proof.

Fix an integer m. Let p = 0, ..., |m|. For each p, define the subsequence

$$r_p[n] = z [n (|m|+1) - p] z [n (|m|+1) - p + m].$$

By Lemma A, $r_p[n]$ is an independent random sequence. Note that

$$0 \le \mathbf{E} \{ r_p[n]^2 \} = \mathbf{E} \{ z [n (|m|+1) - p]^2 \}$$

$$\cdot \mathbf{E} \{ z [n (|m|+1) - p + m]^2 \} < A^4$$

$$0 \le |\mathbf{E} \{ r_p[n] \} | = \left| \mathbf{E} \{ z [n (|m|+1) - p]^2 \} \right|$$

$$\cdot \left| \mathbf{E} \{ z [n (|m|+1) - p + m]^2 \} \right| < A^2.$$

Thus, $0 \leq \operatorname{Var}(r_p[n]) < A^4$ and

р

$$0 \le \sum_{n=1}^{\infty} \frac{\operatorname{Var}(r_p[n])}{n^2} < A^4 \sum_{n=1}^{\infty} \frac{1}{n^2} < \infty.$$
(19)

Given that for each p, $r_p[n]$ is an independent random sequence, the Kolmogorov criterion states that (19) is sufficient to show that $r_p[n]$ obeys the Strong law of large numbers [9]

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} (r_p[n] - \mathbb{E} \{ r_p[n] \}) = 0, \qquad p = 0, \dots, |m|$$
(20)

with probability 1. Summing the |m| + 1 infinite sums in (20) gives

$$\lim_{D \to \infty} \frac{1}{P} \sum_{p=0}^{|m|} \sum_{n=1}^{P} (r_p[n] - E\{r_p[n]\})$$
$$= \lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} (z[n]z[n+m] - R_{zz}[n,m])$$
$$= 0$$

with probability 1. Because $R_{zz}[m]$ exists

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} R_{zz}[n, m] = \overline{R}_{zz}[m]$$

with probability 1.

İ

APPENDIX B

This Appendix presents the derivation of the main theoretical results of this paper. An (L + 1)-level flash ADC, as shown in Fig. 3, is considered. The ideal resistor ladder is driven with reference voltages $+V_{\text{ref}}$ and $-V_{\text{ref}}$, and the ladder provides quantization thresholds $\operatorname{ref}_k = k\Delta - ((L+1)/2)\Delta$, $k = 1, 2, \ldots L$, with a quantization step size $\Delta = (2V_{\text{ref}}/L)$. Each of the L 1-bit ADCs within the flash ADC has an input offset error V_{osk} , $k = 1, 2, \ldots L$.

Let $e(v_{in}, r) = g_{e_q}(v_{in}) + g_{e_{os}}(v_{in}, r)$ be the total error introduced by the flash ADC as a function of the input, where $e_q(v_{in})$ is the error due to ideal (L+1)-level quantization, $e_{os}(v_{in}, r)$ is the error due to 1-bit ADC input offset errors, and $r \in \{-1, 1\}$ is the comparator offset DEM control signal. For the conventional flash ADC, let r[n] = 1, and for a flash ADC with comparator offset DEM, let r[n] be an i.i.d. sequence of random variables with $P\{r = -1\} = P\{r = 1\} = 1/2$.

Let $\alpha_q = 1/\Delta$ denote the effective gain of the flash ADC. Thus, the flash ADC output y[n] is given by

$$y[n] = \alpha_q v_{\rm in}[n] + e[n] \tag{21}$$

where

$$e[n] = e_q[n] + e_{os}[n] = g_{e_q}(v_{in}[n]) + g_{e_{os}}(v_{in}[n], r[n]).$$
(22)

Let the flash ADC input be $v_{in}[n] = x[n] + w[n]$, where x[n] is a deterministic input signal and w[n] is a *dither signal*. It is assumed that x[n] and w[n] are bounded such that $v_{in}[n]$ is within the no-overload range of the quantizer. Let w[n] be an i.i.d. sequence of random variables with $\mu_w = E\{w[n]\}$ and $\sigma_w^2 = E\{w[n]^2\} - \mu_w^2$ for all *n*. Let the characteristic function of w, $\Phi_w(u)$, satisfy the following condition:

$$\Phi_w\left(\frac{2\pi l}{\Delta}\right) = \begin{cases} 1, & l=0\\ 0, & l=\pm 1, \pm 2, \dots \end{cases}$$
(23)

where

$$\Phi_w(u) = \int_{-\infty}^{\infty} f_w(w) e^{juw} \, dw.$$

Provided that $|v_{in}| < V_{ref}$, the use of i.i.d. dither satisfying (6)—e.g., uniform dither on $(-\Delta/2, \Delta/2)$ or triangular dither on $(-\Delta, \Delta)$ —implies that $e_q[n]$ is an i.i.d. sequence of random

variables independent of x[n] and uniformly distributed on $(-\Delta/2, \Delta/2)$ [7], [8].

From (21), the autocorrelation of the flash ADC output is

$$R_{yy}[n, m] = E \{ (\alpha_q v_{in}[n] + e[n]) \\ \cdot (\alpha_q v_{in}[n+m] + e[n+m]) \}.$$
(24)

Expanding $R_{yy}[n, m]$ into its component terms and expressing the expectations as autocorrelations and cross-correlations give

$$R_{yy}[n, m] = \alpha_q^2 R_{v_{in}v_{in}}[n, m] + \alpha_q R_{v_{in}e}[n, m] + \alpha_q R_{ev_{in}}[n, m] + R_{ee}[n, m].$$
(25)

Claims B1–B4 that follow derive expressions for each of the terms on the right-hand side of (25).

Claim B1:

$$R_{v_{\rm in}v_{\rm in}}[n, m] = x[n]x[n+m] + \mu_w x[n] + \mu_w x[n+m] + \mu_w^2 + \delta[m]\sigma_w^2$$
(26)

where

$$\delta[m] = \begin{cases} 1, & m = 0\\ 0, & \text{otherwise.} \end{cases}$$

Proof: Expanding $R_{v_{in}v_{in}}[n, m]$ into its component terms and noting that x[n] is deterministic gives

$$R_{v_{in}v_{in}}[n, m] = x[n]x[n+m] + \mu_w x[n] + \mu_w x[n+m] + E\{w[n]w[n+m]\}.$$
(27)

Because w[n] is i.i.d., $E\{w[n]w[n+m]\} = \mu_w^2 + \delta[m]\sigma_w^2$. Substituting this result into (27) completes the proof. \blacksquare *Claim B2:*

$$R_{v_{in}e}[n, m] = x[n]E\{e_{os}[n+m]\} + \mu_{w}E\{e_{os}[n+m]\} + \delta[m](R_{we_{q}}[n, 0] + R_{we_{os}}[n, 0] - \mu_{w}E\{e_{os}[n]\}).$$
(28)

Proof: Expanding $R_{v_{in}e}[n, m]$ into its component terms and noting that x[n] is deterministic gives

$$R_{v_{in}e}[n, m] = x[n] \mathbb{E} \{ e_q[n+m] \} + x[n] \mathbb{E} \{ e_{os}[n+m] \} + \mathbb{E} \{ w[n] e_q[n+m] \} + \mathbb{E} \{ w[n] e_{os}[n+m] \}.$$
(29)

The first term is zero because $e_q[n]$ is independent of x[n] for all n and has zero mean. By letting $g_n(w, r) = w$ and $h_n(w, r) = g_{e_q}(x[n]+w)$ in Theorem A2, it follows that w[n] and $e_q[n+m]$ are independent for $m \neq 0$. Noting that $e_q[n]$ has zero mean gives

$$E\{w[n]e_q[n+m]\} = \delta[m]E\{w[n]e_q[n]\}.$$
 (30)

By letting $g_n(w, r) = w$ and $h_n(w, r) = g_{e_{os}}(x[n] + w, r)$, it follows from Theorem A2 that w[n] and $e_{os}[n + m]$ are independent for $m \neq 0$ and

_ _ _

$$E \{w[n]e_{os}[n+m]\} = \mu_{w}E \{e_{os}[n+m]\} + \delta[m] \\ \cdot (E\{w[n]e_{os}[n]\} - \mu_{w}E \{e_{os}[n]\}).$$
(31)

Substituting (30) and (31) into (29), expressing the expectations as correlations, and combining the $\delta[m]$ terms completes the proof.

Claim B3: _

$$R_{ev_{in}}[n, m] = x[n+m] \mathbb{E} \{ e_{os}[n] \} + \mu_{w} \mathbb{E} \{ e_{os}[n] \} \\ + \delta[m] \left(R_{we_{q}}[n, 0] + R_{we_{os}}[n, 0] - \mu_{w} \mathbb{E} \{ e_{os}[n] \} \right).$$
(32)

Proof: Because $R_{ev_{in}}[n, m] = E\{e[n]v_{in}[n+m]\}$, this result follows from (28) by letting n' = n + m and m' = -mand by noting that m' = 0 when $\delta[m'] = 1$.

Claim B4:

$$R_{ee}[n, m] = R_{e_{os}e_{os}}[n, m] + \delta[m] \left(E\{e_q^2\} + 2R_{e_qe_{os}}[n, 0] \right).$$
(33)

Proof: Expanding $R_{ee}[n, m]$ into its component terms gives

$$R_{ee}[n, m] = E\{e_q[n]e_q[n+m]\} + E\{e_q[n]e_{os}[n+m]\} + E\{e_{os}[n]e_q[n+m]\} + E\{e_{os}[n]e_{os}[n+m]\}.$$
(34)

Because $e_q[n]$ is i.i.d. and has zero mean, it follows that

$$E\{e_q[n]e_q[n+m]\} = \delta[m]E\{e_q^2\}.$$
 (35)

Note that the n index has been dropped in (35). By letting $g_n(w, r) = g_{e_q}(x[n] + w)$ and $h_n(w, r) = g_{e_{os}}(x[n] + w, r)$, it follows from Theorem A2 that $e_q[n]$ and $e_{os}[n+m]$ are independent for $m \neq 0$ and thus

$$\mathbf{E}\left\{e_{q}[n]e_{\mathrm{os}}[n+m]\right\} = \delta[m]\mathbf{E}\left\{e_{q}[n]e_{\mathrm{os}}[n]\right\}.$$
 (36)

Substituting (35) and (36) into (34), expressing the expectations as correlations, and combining the $\delta[m]$ terms completes the proof.

Claim B5 uses the results of Claims B1-B5 to derive an expression for (25).

Claim B5:

$$R_{yy}[n, m] = \alpha_q^2 x[n] x[n+m] + R'[n, m] + \delta[m] \sigma^2[n] + \mu[n, m]$$
(37)

where

$$R'[n, m] = \alpha_q x[n] \mathbb{E} \{ e_{\rm os}[n+m] \} + \alpha_q x[n+m] \mathbb{E} \{ e_{\rm os}[n] \} + R_{e_{\rm os}e_{\rm os}}[n, m] \quad (38)$$
$$\sigma^2[n] = \alpha^2 \sigma^2 + 2\alpha_s R \quad [n, 0] + 2\alpha_s R \quad [n, 0]$$

$$\sigma^{2}[n] = \alpha_{q}^{2} \sigma_{w}^{2} + 2\alpha_{q} R_{we_{q}}[n, 0] + 2\alpha_{q} R_{we_{os}}[n, 0] - 2\alpha_{q} \mu_{w} \mathbb{E}\{e_{os}[n]\} + \mathbb{E}\{e_{q}^{2}\} + 2R_{e_{q}e_{os}}[n, 0]$$
(39)

and

$$\mu[n, m] = \alpha_q^2 \mu_w x[n] + \alpha_q^2 \mu_w x[n+m] + \alpha_q^2 \mu_w^2 + \alpha_q \mu_w E\{e_{\rm os}[n]\} + \alpha_q \mu_w E\{e_{\rm os}[n+m]\}.$$
(40)

Proof: The results of Claims 1 to 4-(26), (28), (32), and (33)—are applied to the terms of (25). The $\delta[m]$ terms are combined to form $\sigma^2[n]$. The terms dependent on n and m are combined to form R'[n, m]. The remaining terms other than x[n]x[n+m] form $\mu[n, m]$.

In Claims B6-B12 that follow, it is shown that the time-average means and autocorrelations converge to their ensemble values. As stated previously, it is assumed that x[n] and w[n]are bounded to prevent the flash ADC from overloading. Specifically, there exist real numbers X and W such that |x[n]| < Xand $P\{|w[n]| < W\} = 1$ for all n. By definition, $P\{|e_q[n]| \le$ 1/2 = 1, $P\{|e_{os}[n]| \le 1\} = 1$, and $P\{|y[n]| \le L/2\} = 1$. Claim B6:

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} R_{yy}[n, m] = \overline{R}_{yy}[m].$$
(41)

Proof: To show that y[n] satisfies the hypotheses of Theorem A1, let

$$g_n(w, r) = x[n] + w + g_{e_q}(x[n] + w) + g_{e_{os}}(x[n] + w, r).$$

Theorem A1 implies y[n] is a sequence of independent random variables. Because y[n] is bounded and independent, the claim follows from Theorem A4. Claim B7:

n

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} x[n] \mathbb{E} \left\{ e_{\text{os}}[n+m] \right\} = \overline{R}_{xe_{\text{os}}}[m] \qquad (42)$$

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} x[n+m] \mathbb{E} \{ e_{\mathrm{os}}[n] \} = \overline{R}_{e_{\mathrm{os}}} x[m].$$
(43)

Proof: Consider (42) for a fixed value of m, and note that x[n] is a deterministic sequence. Define a new random sequence $z[n] = x[n]e_{os}[n+m]$. To show that z[n] satisfies the hypotheses of Theorem A1, let

$$g_n(w, r) = x[n]g_{e_{os}}(x[n+m]+w, r).$$

Theorem A1 implies that z[n] is independent. Because x[n] and $e_{cs}[n]$ are bounded, $P\{|z[n]| \le X\} = 1$. By Theorem A3

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} x[n] \mathbb{E} \{ e_{\text{os}}[n+m] \}$$
$$= \lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} x[n] e_{\text{os}}[n+m] = \overline{R}_{xe_{\text{os}}}[m].$$

Thus (42) holds. The equality in (43) follows by the same reasoning with $z[n] = x[n+m]e_{os}[n]$. Claim B8:

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} R_{e_{\rm os}} e_{\rm os}[n, m] = \overline{R}_{e_{\rm os}} e_{\rm os}[m].$$

Proof: To show that $e_{os}[n]$ satisfies the hypotheses of Theorem A1, let

$$g_n(w, r) = g_{e_{os}}(x[n] + w, r)$$

Theorem A1 implies that $e_{os}[n]$ is independent. Because $e_{os}[n]$ is bounded, the claim follows from Theorem A4. Claim B9:

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} R_{we_q}[n, 0] = \overline{R}_{we_q}[0]$$

Proof: Define a new random sequence $z[n] = w[n]e_q[n]$. To show that z[n] satisfies the hypotheses of Theorem A1, let

$$g_n(w, r) = x[n]g_{e_q}(x[n+m]+w).$$

Theorem A1 implies that z[n] is independent. Because w[n] and $e_q[n]$ are bounded, $P\{|z[n]| \le W/2\} = 1$. By Theorem A3

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} \mathbb{E}\{w[n]e_q[n]\}$$
$$= \lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} w[n]e_q[n] = \overline{R}_{we_q}[0].$$

Claim B10:

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} R_{we_{os}}[n, 0] = \overline{R}_{we_{os}}[0].$$

Proof: Define a new random sequence $z[n] = w[n]e_{os}[n]$. To show that z[n] satisfies the hypotheses of Theorem A1, let

$$g_n(w, r) = x[n]g_{e_{os}}(x[n+m]+w, r).$$

Theorem A1 implies z[n] is independent. Because w[n] and $e_{os}[n]$ are bounded, $P\{|z[n]| \le W\} = 1$. By Theorem A3

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} \mathrm{E}\{w[n]e_{\mathrm{os}}[n]\} \\= \lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} w[n]e_{\mathrm{os}}[n] = \overline{R}_{we_{\mathrm{os}}}[0]$$

Claim B11:

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} \mathrm{E}\{e_{\mathrm{os}}[n]\} = \overline{M}_{e_{\mathrm{os}}}.$$

Proof: As shown in Claim B8, $e_{os}[n]$ is independent and bounded. The claim then follows from Theorem A3. *Claim B12:*

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} R_{e_q e_{os}}[n, 0] = \overline{R}_{e_q e_{os}}[0].$$

Proof: Define a new random sequence $z[n] = e_q[n]e_{os}[n]$. To show that z[n] satisfies the hypotheses of Theorem A1, let

$$g_n(w, r) = g_{e_q}(x[n] + w)g_{e_{os}}(x[n] + w, r).$$

Theorem A1 implies z[n] is independent. Because $e_q[n]$ and $e_{\rm os}[n]$ are bounded, $P\{|z[n]| \le 1\} = 1$. By Theorem A3

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} \mathbb{E}\{e_q[n]e_{\rm os}[n]\}$$
$$= \lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} e_q[n]e_{\rm os}[n] = \overline{R}_{e_q e_{\rm os}}[0].$$

Given the results of the preceding claims, the main theoretical results of this paper can now be stated.

Claim B13: The autocorrelation of the flash ADC output is given by

$$\overline{R}_{yy}[m] = \alpha_q^2 \overline{R}_{xx}[m] + \overline{R}'[m] + \overline{\sigma}^2 \delta[m] + \overline{\mu}$$
(44)

where

$$\overline{R}'[m] = \alpha_q \overline{R}_{xe_{os}}[m] + \alpha_q \overline{R}_{e_{os}x}[m] + \overline{R}_{e_{os}e_{os}}[m] \quad (45)$$
$$\overline{\sigma}^2 = \alpha^2 \sigma_{x}^2 + 2\alpha_q \overline{R}_{we} \quad [0] + 2\alpha_q \overline{R}_{we} \quad [0]$$

$$= \alpha_q^2 \sigma_w^2 + 2\alpha_q R_{we_q}[0] + 2\alpha_q R_{we_{os}}[0] - 2\alpha_q \mu_w \overline{M}_{e_{os}} + \mathbb{E}\{e_q^2\} + 2\overline{R}_{e_q e_{os}}[0]$$
(46)

$$\overline{\mu} = 2\alpha_q^2 \mu_w \overline{M}_x + \alpha_q^2 \mu_w^2 + 2\alpha_q^2 \mu_w \overline{M}_{e_{\rm os}}.$$
(47)

The PSD of the flash ADC output is given by

$$S_{yy}(e^{j\omega}) = \alpha_q^2 S_{xx}(e^{j\omega}) + S'(e^{j\omega}) + \overline{\sigma}^2 + \overline{\mu}\,\delta(e^{j\omega}) \quad (48)$$

where

$$S'(e^{j\omega}) = \sum_{m=-\infty}^{\infty} \overline{R}'[m]e^{-j\omega m}.$$
 (49)

Proof: Taking time averages of (37)–(40), using the results of Claims B6–B12, and combining terms yields (44)–(47). The PSD results in (48) and (49) follow from the definition in (17) by taking the Fourier transform of each of the terms in (44).

REFERENCES

- E. Fogleman, I. Galton, W. Huff, and H. Jensen, "A 3.3-V single-poly CMOS audio ADC delta-sigma modulator with 98-dB peak SINAD and 105-dB peak SFDR," *IEEE J. Solid-State Circuits*, vol. 35, pp. 297–307, Mar. 2000.
- [2] G. Lainey, R. Saintlaurens, and P. Senn, "Switched-capacitor secondorder noise-shaping coder," *Electron. Lett.*, vol. 19, pp. 149–150, Feb. 1983.
- [3] I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters," *IEEE Trans. Circuits Syst. II*, vol. 44, pp. 808–817, Oct. 1997.
- [4] E. Fogleman, I. Galton, and H. Jensen, "An area-efficient differential input ADC with digital common mode rejection," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 2, June 1999, pp. 347–350.
- [5] R. Gregorian, Introduction to CMOS OP-AMP's and Comparators. New York: Wiley, 1999, pp. 198–199.
- [6] I. Galton, "Granular quantization noise in a class of delta-sigma modulators," *IEEE Trans. Inform. Theory*, vol. 40, pp. 848–859, May 1994.
- [7] L. Schuchman, "Dither signals and their effects on quantization noise," *IEEE Trans. Commun. Technol.*, vol. COM-12, pp. 162–165, Dec. 1964.
- [8] A. B. Sripad and D. L. Snyder, "A necessary and sufficient condition for quantization errors to be uniform and white," *IEEE Trans. Acoust.*, *Speech, Signal Processing*, vol. ASSP-25, pp. 442–448, Oct. 1977.
- [9] W. Feller, An Introduction to Probability Theory and Its Applications, 3rd ed. New York: Wiley, 1950, vol. I.



Eric Fogleman received the B.S. degree in electrical engineering from the University of Maryland, College Park, in 1990 and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of California, San Diego (UCSD), in 1998 and 2000, respectively.

From 1990 to 1993, he was with Analog Devices, Wilmington, MA as a Product/Test Engineer for audio converter products. From 1993 to 1996, he was with Brooktree Corp., San Diego, CA, as a Product Engineer and Design Engineer for computer audio

and multimedia graphics products. From 1996 to 2000, he was a Graduate Student Researcher at UCSD. In 2000, he worked for Broadcom Corporation, Irvine, CA, as a Design Engineer. He currently works for Silicon Wave, San Diego, CA, as a Design Engineer. His interests are in mixed-signal circuit design and signal processing.



Ian Galton (M'92) received the Sc.B. degree from Brown University, Providence, RI, in 1984 and the M.S. and Ph.D. degrees from the California Institute of Technology, Pasadena, in 1989 and 1992, respectively, all in electrical engineering.

He is currently an Associate Professor at the University of California, San Diego. He was formerly with UC Irvine, Acuson, and Mead Data Central, and has acted as a regular consultant for several companies. His research interests involve integrated circuits and systems for communications

including ADCs, DACs, frequency-to-digital converters, frequency synthesizers, synchronization and offset removal blocks for digital modems, and receiver linearization circuits.photography and biography not available at time of publication.