A Digital Common-Mode Rejection Technique for Differential Analog-to-Digital Conversion

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***Abstract*—A multibit $\Delta\Sigma$ analog-to-digital converter can achieve high resolution with a lower order $\Delta\Sigma$ modulator and lower oversampling ratio than a single-bit design, but it requires a multibit internal flash analog-to-digital converter rather than a simple comparator. In an implementation with a fully differential analog front end, the flash analog-to-digital converter must quantize a differential voltage relative to a set of differential reference voltages. Though analog techniques for differential analog-to-digital conversion exist, implementing them in a low-voltage single-poly CMOS process is a challenging circuit design problem. This paper presents a digital common-mode rejection technique for differential analog-to-digital conversion (ADC), which avoids the circuit complexity and die area requirements of analog common-mode rejection techniques. This technique was used to implement the internal quantizer in two high-performance single-poly CMOS ADC $\Delta\Sigma$ modulator prototypes with over 98-dB peak signal-to-noise-and-distortion ratio and 105-dB spurious-free dynamic range. Implementation details, die area requirements, and measured common-mode rejection are presented for the prototype. Signal-processing details of digital common-mode rejection within the $\Delta\Sigma$ modulator are presented, showing that injected common-mode noise results only in modulation of the quantization error power and does not create spurious tones.**

***Index Terms*—Analog circuits, analog–digital conversion, CMOS analog integrated circuits, mixed analog–digital integrated circuits, sigma–delta modulation.**

I. Introduction

THE DEVELOPMENT of mismatch-shaping multibit digital-to-analog converters (DACs) has helped make the implementation of high-resolution multibit $\Delta\Sigma$ analog-to-digital converters (ADCs) feasible. Compared to a single-bit design, a multibit $\Delta\Sigma$ ADC can achieve the same signal-to-quantization-noise performance with a lower $\Delta\Sigma$ modulator order and lower oversampling ratio. The use of multibit feedback also relaxes the slew rate and settling time requirements on the analog integrators by greatly reducing the magnitude of the error signal to be integrated.

While reducing the $\Delta\Sigma$ modulator order and oversampling ratio eases the design of the analog front end, it also reduces the noise transfer function's attenuation of circuit noise introduced at the quantizer. Thus the performance of the internal quantizer, typically implemented as a flash ADC, can limit the $\Delta\Sigma$ modulator's performance. High-performance $\Delta\Sigma$ADCs use fully differential analog circuitry to improve their immunity to noise coupled through the bias nodes, power supplies, and substrate. To preserve the noise rejection benefits of the differential architecture, the flash ADC must quantize the loop filter's differential output and reject its common-mode component.

Conventional analog circuit techniques for implementing differential input flash ADCs present significant design challenges in a 3.3-V single-poly CMOS process optimized for digital circuits. One approach uses a pair of switched capacitors per comparator to sample the input and reference levels on alternating clock phases [1], [2]. This technique can require a prohibitively large area for a multibit $\Delta\Sigma$ modulator implemented in a CMOS process in which large-area metal–metal capacitors are the only linear capacitor structures. Because the reference ladder is sampled in the switched-capacitor approach, its design is complicated by the requirement that the capacitors must be fully charged at the oversampled clock rate. An alternate common-mode rejection circuit, referred to as a differential differencing amplifier (DDA), uses two differential pairs per comparator to subtract the common-mode component in the current domain [3]. This approach is challenging given the limited supply voltage because it requires the design of a differential pair with a wide linear input range, low input-referred offset, and high transconductance. In addition, modulation of the differential pairs' transconductances by the common-mode signal can give rise to intermodulation of the differential-mode signal and the common-mode noise.

This paper presents a digital common-mode rejection (DCMR) flash ADC and noise-shaped requantizer used as the internal quantizer in a pair of high-performance single-poly CMOS $\Delta\Sigma$ modulator IC prototypes [4], [5]. The DCMR flash ADC and requantizer together perform 33-level differential mode quantization without the area penalty and circuit complications of the switched-capacitor or DDA approaches. The DCMR flash ADC uses a pair of single-ended 33-level flash ADCs to quantize the positive and negative portions of the loop filter's differential output and digitally subtracts the single-ended outputs to cancel the common-mode component. Because the subtraction results in a 65-level difference signal, a dithered, first-order shaped requantizer reduces the DCMR flash ADC output to 33 levels. The requantizer allows the use of a 33-level mismatch-shaping DAC encoder rather than a more complex 65-level encoder. Theoretical results are presented

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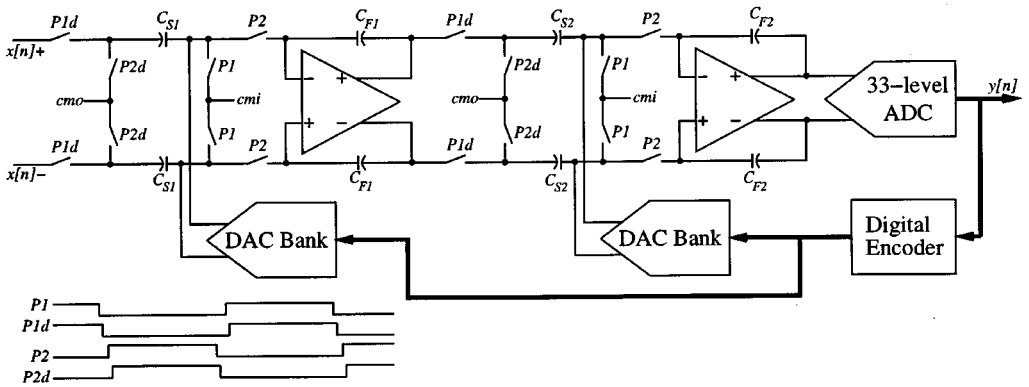

Fig. 1. The high-level circuit topology of the prototype ADC $\Delta\Sigma$ modulator.

that show that the DCMR flash ADC provides a quantized representation of the differential signal with quantization error power less than or equal to that of a conventional 33-level flash ADC even in the presence of common-mode noise. The prototype implementation details show that the DCMR flash ADC required less area than the switched-capacitor and DDA implementations considered for the prototype. The measured common-mode rejection performance of the prototype shows that the DCMR flash ADC can reject a 200-mV common-mode sinusoid with only 0.4-dB degradation in the $\Delta\Sigma$ modulator's signal-to-noise-and-distortion ratio.

This paper consists of two main sections and an Appendix. Section II presents the implementation of the DCMR flash ADC in the ADC $\Delta\Sigma$ modulator prototype IC initially presented in [4], simulated common-mode rejection of the DCMR flash ADC, and measured common-mode rejection of the DCMR flash ADC in the prototype IC. Section III presents the signal-processing details of the DCMR flash ADC and noise-shaped requantizer used within a multibit $\Delta\Sigma$ modulator. The Appendix presents detailed derivations of results used in Section III.

II. DCMR Implementation in the $\Delta\Sigma$ Modulator Prototype

The $\Delta\Sigma$ modulator described in the introduction is a second-order design operating at a clock rate of 3.072 MHz with an oversampling ratio of 64. The prototype was fabricated in a 3.3-V 0.5-μm single-poly triple-metal CMOS process, and it achieves 98-dB peak signal-to-noise-and-distortion (SINAD) and 105-dB spurious-free dynamic range (SFDR) in a 24-kHz signal bandwidth [4]. As shown in Fig. 1, it was implemented with two delaying switched-capacitor integrators, a 33-level mismatch-shaping DAC, and a 33-level DCMR flash ADC [4], [6], [7]. The single-ended flash ADCs within the DCMR flash ADC use a comparator offset dynamic element matching (DEM) technique to attenuate distortion caused by comparator input offset errors [8].

While the $\Delta\Sigma$ modulator's noise transfer function does provide some attenuation of circuit noise introduced at the quantizer, it provides only 52 dB of attenuation at the 24-kHz passband edge. For example, if the common-mode to differential-mode conversion gain ($A_{\mathrm{cm-dm}}$) of flash ADCs input stage is 0 dB, the converter's common-mode rejection ratio (CMRR) will be 54 dB at 24 kHz and at multiples of 3.072 MHz $\pm$ 24 kHz. In this case, a 30-mV 24-kHz common-mode sinusoid at the quantizer's input will limit the $\Delta\Sigma$ADC's peak SFDR to 82 dB. Thus, the quantizer must provide additional common-mode rejection to preserve the benefits of the fully differential analog front end and to ensure meeting the 105-dB SFDR target.

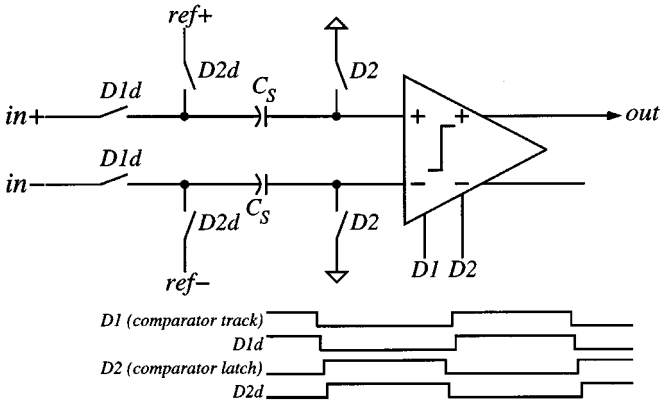

Fig. 2. The switched-capacitor common-mode rejection approach applied to a comparator within the flash ADC.

A. Conventional Approaches

Two conventional approaches to implementing a 33-level, differential input flash ADC were considered for the $\Delta\Sigma$ modulator prototype, but the die area requirements and circuit design challenges motivated the search for an alternative solution.

The switched-capacitor common-mode rejection approach, shown in Fig. 2, uses a pair of switched capacitors for each comparator in the flash ADC to sample the differential input signal, $(\mathrm{in}_+ - \mathrm{in}_-)$, and differential reference, $(\mathrm{ref}_+ - \mathrm{ref}_-)$, on alternate clock phases [1]. A 33-level switched-capacitor flash ADC would require a bank of 32 comparators, an array of 64 capacitors, and a 33-level thermometer-to-binary decoder. To keep the sampling capacitor large relative to the comparators' input capacitance, it must be on the order of 100 fF. With the

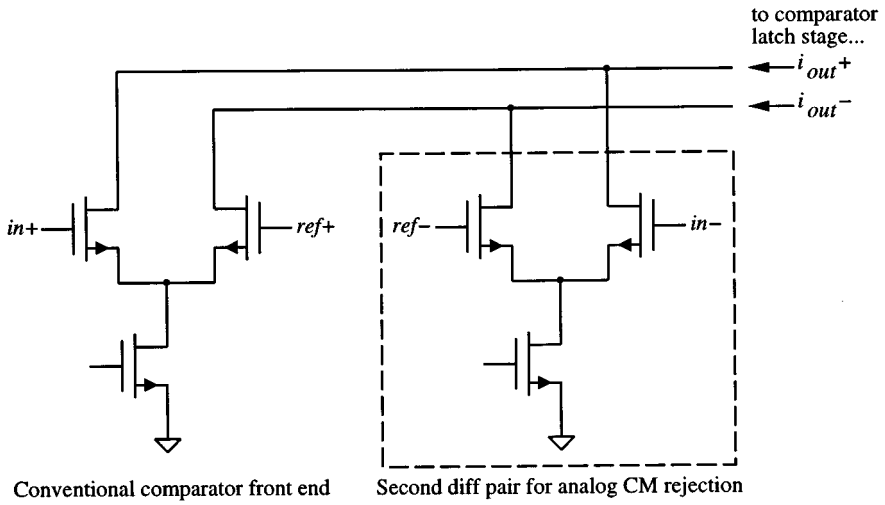

Fig. 3. DDA common-mode rejection applied to a comparator within the flash ADC.

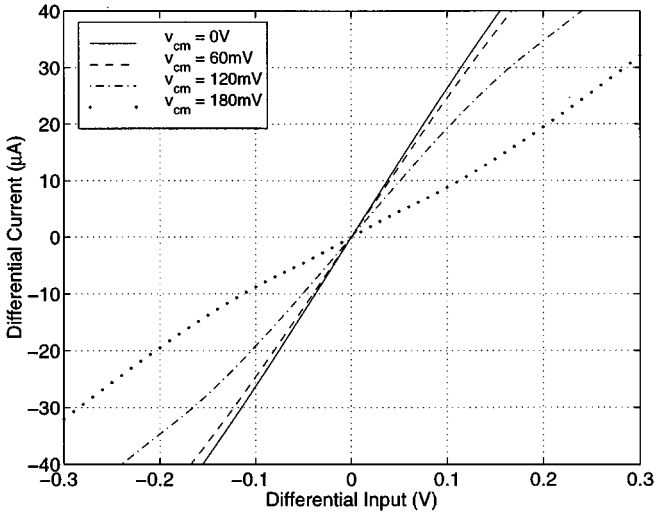

Fig. 4. Simulation results illustrating the modulation of the DDA transconductance by the common-mode signal.

parallel-plate metal interconnect capacitors used in the design, the sampling capacitor array would have required an area of approximately 0.40 mm^2. Thus, the sampling capacitors would have dominated the 0.59-mm^2 total die area required for the flash ADC with switched-capacitor common-mode rejection. In addition, each of the 32 sampling capacitors would have a bottom-plate parasitic capacitance to the substrate on the order of 50–100 fF. These parasitic capacitances would be switched between the second integrator's output and the reference ladder on alternate clock phases, so the reference ladder would need to be capable of fully charging them to avoid signal-dependent settling errors that would give rise to distortion. The references' source resistance could have been reduced by using low resistance values in the ladder, but this would have increased power dissipation and required fast-settling, high current buffers to drive the ends of the resistor ladder. Source-followers could have been used on each reference tap to reduce the source resistance as in [9], but threshold voltage mismatches among devices would have introduced an additional distortion mechanism.

The DDA approach, shown in Fig. 3, uses two differential pairs per comparator to convert the signals $(\mathrm{in}_+ - \mathrm{ref}_+)$ and $(\mathrm{in}_- - \mathrm{ref}_-)$ to currents which are subtracted to reject the common-mode component [3]. The challenge in implementing this technique is that the differential pairs must have a sufficiently wide linear input range to accommodate the expected common-mode offset and common-mode noise. For a fixed tail current, increasing the input range would imply reduced transconductance and reduced attenuation of offsets in the latching stage. For a fixed transconductance, increasing the input range would imply increased tail current and thus increased power dissipation. A second problem results from the modulation of the differential pairs' transconductance by the input common-mode level. Fig. 4 shows the differential output current of a DDA input stage as a function of the differential input voltage for several common-mode levels. In this simulation, $(\mathrm{ref}_+ - \mathrm{ref}_-) = 0$ V. The change in slope near zero differential input indicates the degree of change in the transconductance. In a comparator, this effect would cause the input-referred offset of the latching stage to be modulated by the common-mode signal and would lead to a mechanism for the intermodulation of the common-mode and differential-mode signals.

Though it would be possible to use the comparator offset dynamic element matching (DEM) technique presented with the DDA approach to spectrally whiten the effects of static offsets due to the differential pairs and latching stage, the offsets dependent on the common-mode signal could still lead to spurious tones. Therefore, with the DDA approach, it is best to use large-area well-matched devices to minimize the magnitude of these signal-dependent offsets. Thus, even though the DDA approach does not require capacitors, it would result in increased die area because minimum-size devices could not be used in the 32 comparators [10].

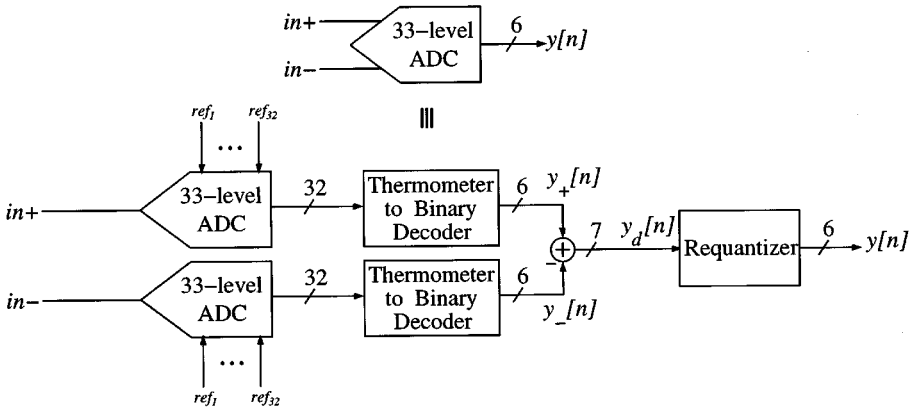

Fig. 5. The high-level circuit topology of the digital common-mode rejection flash ADC architecture.

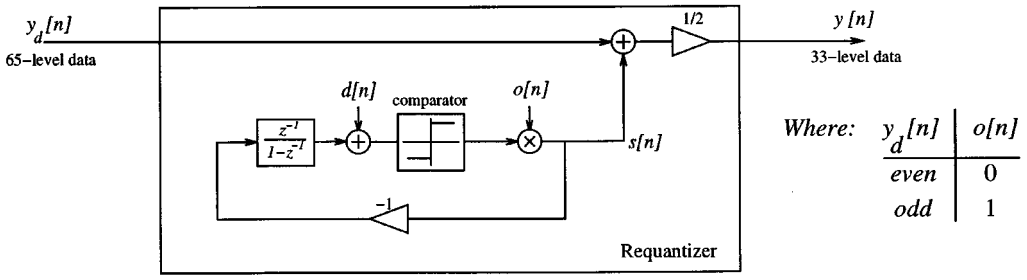

Fig. 6. Signal processing performed by the noise-shaped requantizer.

B. The DCMR Approach

The DCMR flash ADC, shown in Fig. 5, was implemented in the $\Delta\Sigma$ modulator to avoid the area requirements and circuit difficulties of the conventional approaches described above. The DCMR flash ADC implemented in the $\Delta\Sigma$ modulator prototype uses a pair of 33-level single-ended flash ADCs with a shared reference ladder to quantize the positive and negative portions of the second integrator's differential output.

In the absence of common-mode noise, the DCMR flash ADC output would take on only even values, and the least significant bit (LSB) could simply be dropped to yield a 33-level quantized representation of the differential input. However, when common-mode noise is present, the difference signal takes on both even and odd values. One could use a 65-level mismatch-shaping DAC encoder rather than a 33-level encoder to accommodate the additional quantization levels, but this would nearly double its die area. Truncating the LSB in this case to yield a 33-level signal would create spurious tones because truncation is a form of undithered quantization. To reduce $y_d[n]$ to 33 levels without introducing spurious tones, the noise-shaped requantizer shown in Fig. 6 was used. As will be shown in Section III, the requantization error can spectrally shaped by generating a *switching sequence*, $s[n]$, with the desired power spectral density (PSD). The circuit in Fig. 6 that generates $s[n]$ is analogous to a dithered first-order digital $\Delta\Sigma$ modulator with zero input, and it produces a switching sequence with a first-order high-pass-shaped PSD. The signal $o[n]$ represents the parity of $y_d[n]$, and the multiplier controlled by $o[n]$ forces $s[n] = 0$ when $y_d[n]$ is even. The comparator in Fig. 6 outputs $+1$ for inputs greater than zero and -1 otherwise. The dither signal $d[n]$ is an independent identically distributed (i.i.d.) sequence of random variables with a uniform distribution on $(-1/2,\ 1/2]$ that is used to decorrelate $s[n]$ from $y_d[n]$.

The noise-shaped requantizer's signal processing is identical to that of the first-order switching block in the mismatch-shaping DAC encoder presented in [6]. This allowed the same hardware simplifications used in the mismatch-shaping DAC encoder of [4] to be applied in the gate-level implementation of the requantizer, shown in Fig. 7. The parity of $y_d[n]$ is given by its LSB, $y_d^{(0)}[n]$. The dither signal $r[n]$ is an i.i.d. sequence of random variables taking values of zero and one with equal probability. The E inputs of the D flip-flops are enable signals that inhibit the state update when $y_d[n]$ is even, and *CLK* is a clock signal at the sample rate. Taken as a pair, the signals $q[n]$ and $y_d^{(0)}[n]$ in Fig. 7 form a sign/magnitude representation of the switching sequence $s[n]$. With this simplified hardware implementation, the noise-shaped requantizer requires only 17 logic gates and two D-flip-flops.

By avoiding the use of capacitors, the DCMR approach eliminates the area overhead of the metal–metal capacitors needed to implement switched-capacitor common-mode rejection. While both the DDA common-mode rejection approach and the DCMR approach require 64 differential pairs, these devices can be made nearly minimum-size in the DCMR flash ADC if comparator offset DEM is used to spectrally whiten the input-referred offsets of each comparator [8]. This advantage offsets the fact that the DCMR flash ADC requires additional digital logic—a second 33-level thermometer-to-binary encoder, an adder, and requantization logic.

Behavioral simulation results for the $\Delta\Sigma$ modulator with a -6-dB sinusoidal input are shown in Fig. 8. In the absence of common-mode noise, the $\Delta\Sigma$ modulator achieves 101.9-dB

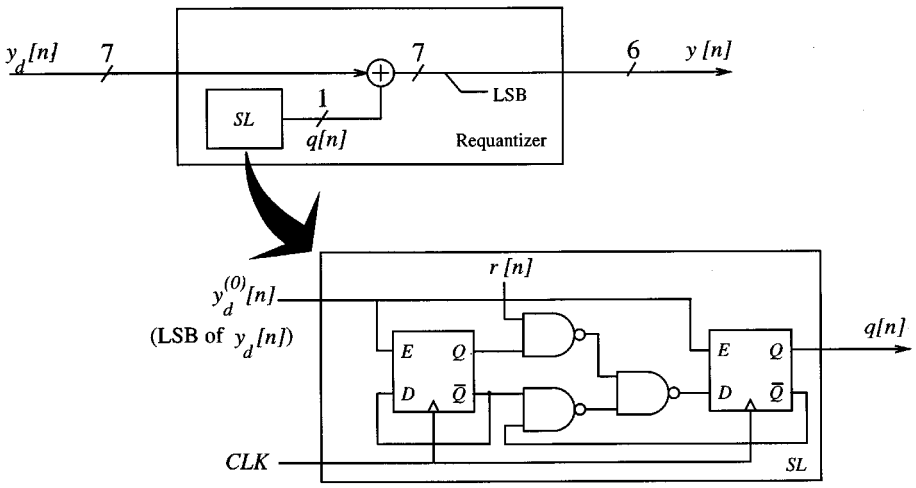

Fig. 7. Gate-level implementation of the noise-shaped requantizer.

SINAD, as shown in the PSD plot in Fig. 8(a). Fig. 8(b)–(d) shows simulated performance with a 200-mV peak, 20.7-kHz common-mode sinusoid superimposed on the second integrator's output. The PSD for the $\Delta\Sigma$ modulator using a single-ended flash ADC with no common-mode rejection is shown in Fig. 8(b) to emphasize that the noise-transfer function alone does not provide sufficient attenuation to ensure meeting the 105-dB SFDR target. In this case, the SINAD is limited to 56.9 dB by the 20.7-kHz spurious component. Fig. 8(c) shows the output PSD when the DCMR flash ADC is used and the difference signal is reduced to 33 levels by truncation. As noted previously, undithered truncation generates significant spurious tones. The configuration used in the $\Delta\Sigma$ modulator prototype—the DCMR flash ADC and the dithered first-order shaped requantizer—is shown in Fig. 8(d). Despite the presence of a significant common-mode signal, the $\Delta\Sigma$ modulator achieves 104.1-dB SINAD. As will be shown in the next section, the presence of common-mode noise can in some cases *reduce* the quantization error power in the DCMR flash ADC.

Measured common-mode rejection results for the $\Delta\Sigma$ modulator prototype IC in Fig. 9 show that the DCMR flash ADC effectively eliminates common-mode noise. With -6-dB 1.5-kHz input and no common-mode noise, as shown in Fig. 9(a), the SINAD is 96.2 dB. With a 200-mV peak, 20.7-kHz sinusoid injected on the flash ADC's reference ladder, as shown in Fig. 9(b), the SINAD is 95.8 dB. The SFDR in each case is 110.8 dB and is limited by the third-harmonic distortion of the switched-capacitor circuitry rather than the performance of the DCMR flash ADC.

By avoiding the use of capacitors, the DCMR flash ADC resulted in significant area savings in a single-poly CMOS implementation. Fig. 10 shows the layout of the prototype $\Delta\Sigma$ modulator using the DCMR flash ADC and requantizer presented in [5]. The 33-level DCMR flash ADC die area in a 0.5-μm[1] single-poly CMOS process is 0.42 mm^2. Even though switched-capacitor common-mode rejection would have reduced the number of comparators by a factor of two, it would have required a 0.40-mm^2 capacitor array—approximately the size of C_{DAC_2} in Fig. 10—making its total area 0.59 mm^2. Thus, the DCMR approach provided a 30% reduction in die area relative to the switched-capacitor approach.

The die area of the DCMR flash ADC also compares favorably to that required for the DDA approach. In [10], a 17-level flash ADC was implemented in a 0.65-μm CMOS process using the DDA approach with a die area of approximately 0.22 mm^2. Assuming that extending this design to 33 levels would double its area, this design would require roughly the same area as the DCMR flash ADC. As future generations of CMOS fabrication processes are developed with even smaller device dimensions and further reduced supply voltages, the DCMR approach will be even more attractive because it minimizes the requirements on the analog circuits and capitalizes on the strengths of a digital-optimized fabrication process.

III. Signal Processing Details

Each single-ended flash ADC within the DCMR flash ADC is implemented as shown in Fig. 11. The *positive flash ADC* quantizes the positive half of the second integrator's differential output, and the *negative flash ADC* quantizes the negative half of the differential output. Each flash ADC implements a mid-step quantizer with step size $\Delta/2$, where Δ is the step size of the overall DCMR flash ADC. Let $g_{y+}(v)$ denote the input–output transfer function of the positive flash ADC, where the output sequence is $y_+[n] = g_{y+}(v[n])$. The input–output transfer function is given by

$$g_{y+}(v) = \frac{1}{\Delta/2}\, v + g_{e_{q+}}(v) \tag{1}$$

and the quantization error is given by

$$g_{e_{q+}}(v) = \frac{1}{2} - \left\langle \frac{v}{\Delta/2} + \frac{1}{2} \right\rangle \tag{2}$$

[1]Minimum drawn gate length in this process is 0.6 μm.

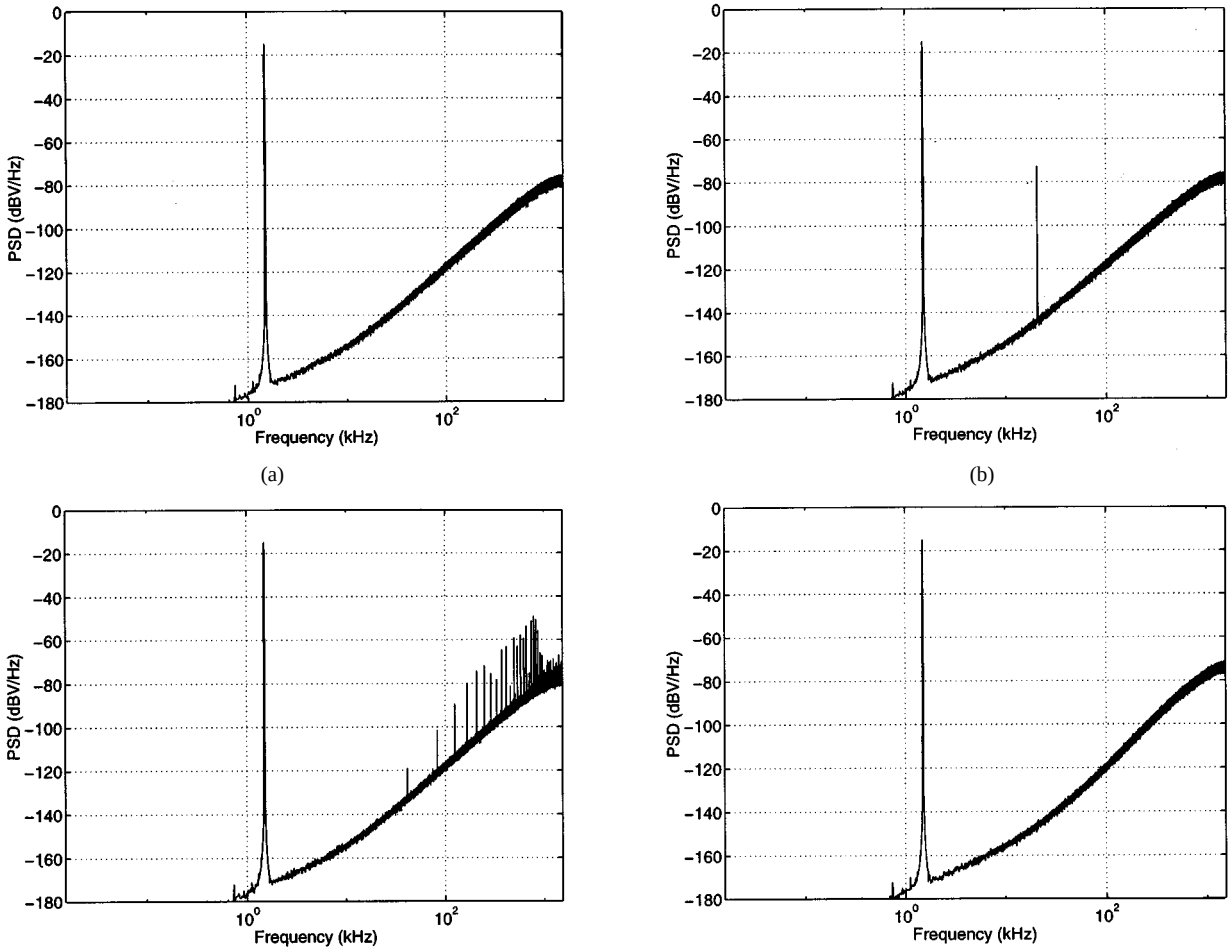

Fig. 8. Comparison of simulated results for a -6-dB 1.5-kHz input signal and 200-mV 20.7-kHz common-mode noise. (a) No common-mode noise, (b) no common-mode rejection, (c) DCMR with truncation, and (d) DCMR with shaped requantization.

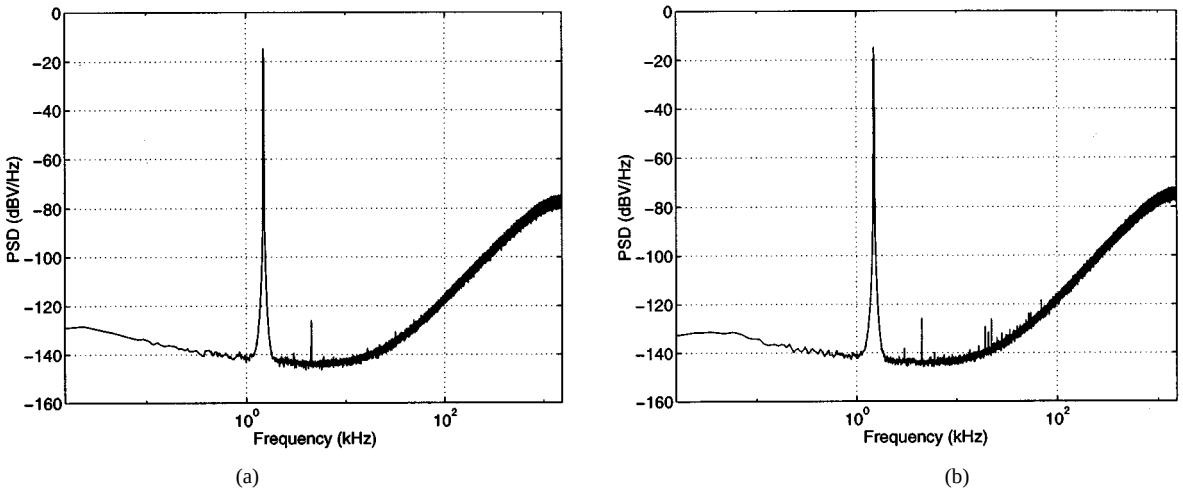

Fig. 9. Measured performance of DCMR in the $\Delta\Sigma$ modulator prototype. (a) No common-mode noise and (b) 200-mV peak 20.7-kHz common-mode sinusoid injected on reference ladder to flash ADCs.

where $\langle x \rangle$ denotes the fractional part of x. Similarly, the negative flash ADC's input–output transfer function is given by

$$g_{y-}(v) = \frac{1}{\Delta/2} v + g_{e_{q-}}(v) \tag{3}$$

where

$$g_{e_{q-}}(v) = -\frac{1}{2} + \left\langle -\frac{v}{\Delta/2} + \frac{1}{2} \right\rangle. \tag{4}$$

For convenience in the analysis that follows, the values of (1) and (3) at the quantization thresholds have been assigned differ-

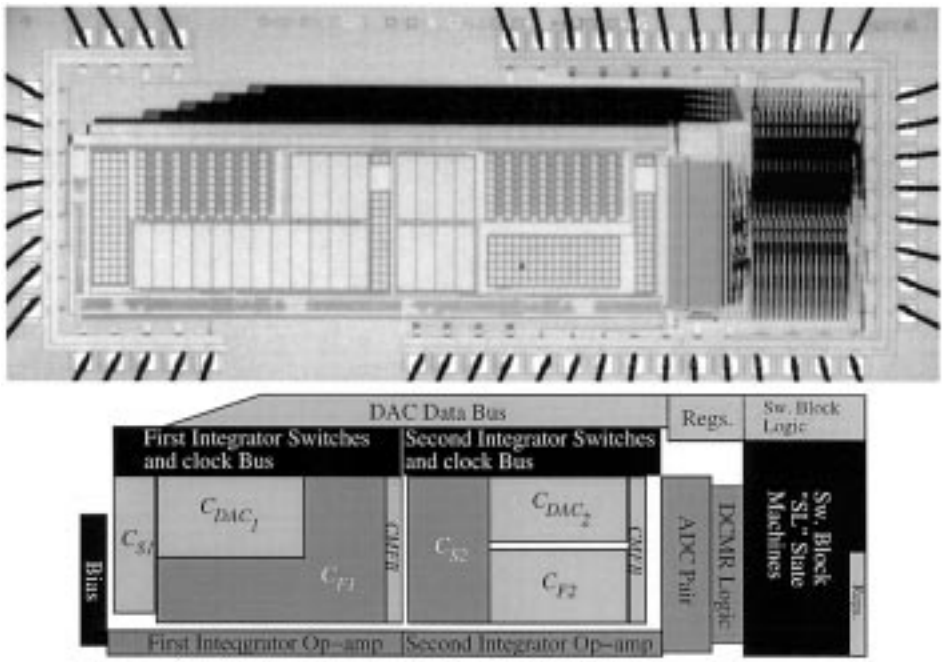

Fig. 10. Layout of the 33-level DCMR flash ADC within the $\Delta\Sigma$ modulator prototype.

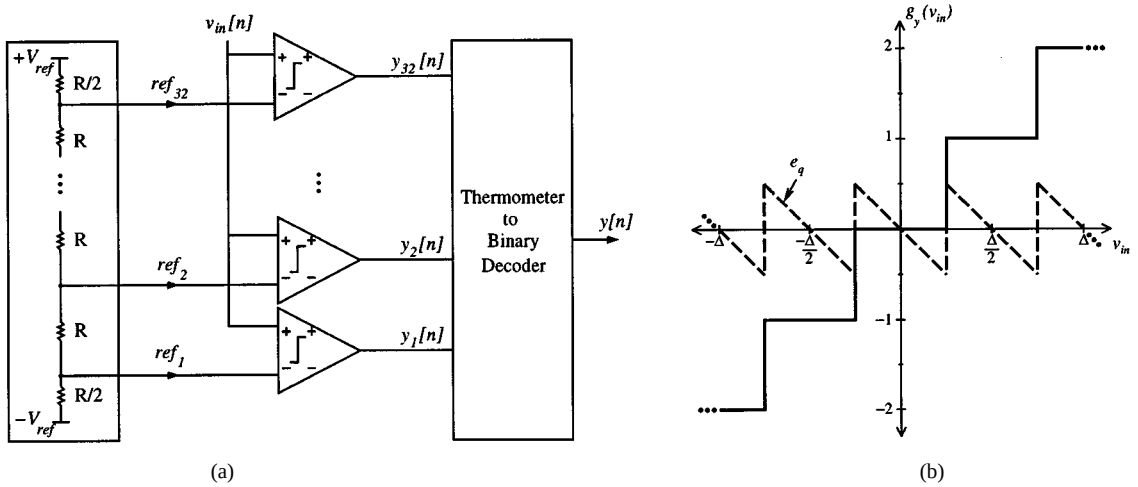

Fig. 11. (a) Single-ended flash ADC. (b) Transfer function of single-ended flash ADC.

ently. For physical analog signals, the probability of the input's landing exactly on a quantization threshold is zero. Therefore, this choice does not affect the final results.

Let $v_{\rm in}$ denote the DCMR flash ADC's differential-mode input signal, and let $v_{\rm cm}$ denote its common-mode input signal. The DCMR flash ADC's input–output transfer function $g_{y_d}(v_{\rm in}, v_{\rm cm})$ is formed by subtracting the outputs of the positive and negative flash ADCs and is given by

$$g_{y_d}(v_{\rm in}, v_{\rm cm}) = \frac{2v_{\rm in}}{\Delta} + g_{e_{q+}}\left(\frac{v_{\rm in}}{2} + v_{\rm cm}\right) - g_{e_{q-}}\left(-\frac{v_{\rm in}}{2} + v_{\rm cm}\right) \quad (5)$$

where $g_{e_{q+}}(v)$ and $g_{e_{q-}}(v)$ are given by (2) and (4), respectively.

Figs. 12–14 show how the common-mode signal affects the quantization error at the output of the DCMR flash ADC. In Fig. 12, $v_{\rm cm} = 0$, and the resulting quantization error is that of a 33-level quantizer followed by a gain of two. As noted previously, the DCMR flash ADC produces only even outputs when $v_{\rm cm} = 0$. As the common-mode voltage is increased to $\Delta/16$, as shown in Fig. 13, the positive flash ADC's transfer function moves to the left and the negative flash ADC's transfer function moves to the right. Though this results in nonuniform quantization, the input–output transfer function is still a periodic function of $v_{\rm in}$ with period Δ. For $v_{\rm cm} = \Delta/8$, as in Fig. 14, the DCMR flash ADC's transfer function is effectively that of a 65-level quantizer. Thus, a side-effect of the DCMR flash ADC is that the correlation between the error of the positive and negative flash ADCs tends to reduce the overall quantization error for inputs with a nonzero common-mode component.

Because of the relationship between the quantization errors noted above, the negative flash ADC's quantization error

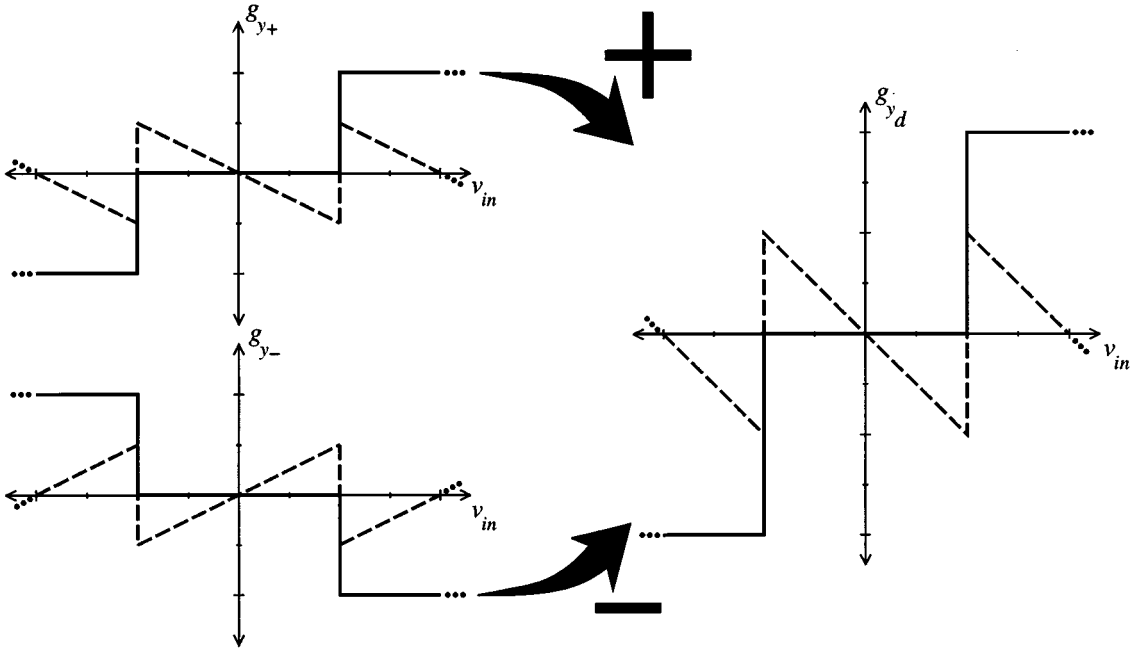

Fig. 12. DCMR flash ADC output and quantization error transfer functions with $v_{\rm cm} = 0$.

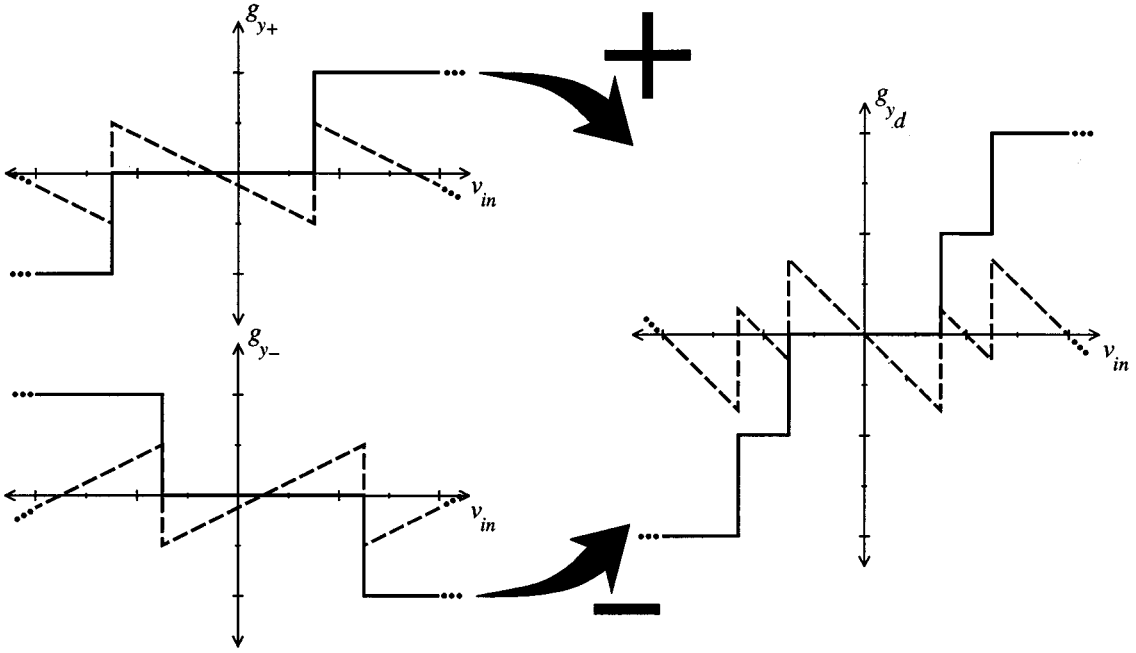

Fig. 13. DCMR flash ADC output and quantization error transfer functions with $v_{\rm cm} = \Delta/16$.

is completely determined given the positive flash ADC's quantization error and the common-mode signal according to

$$g_{e_{q-}}(e_{q+}, v_{\rm cm}) = -\frac{1}{2} + \left\langle -e_{q+} - \left\langle \frac{4v_{\rm cm}}{\Delta} \right\rangle \frac{1}{2} \right\rangle \quad (6)$$

where e_{q+} is the quantization error of the positive flash ADC. Thus, the quantization error of the DCMR flash ADC can be viewed as a memoryless transformation of the positive flash ADC's quantization error, which depends on the common-mode signal with

$$g_{e_{q_d}}(e_{q+}, v_{\rm cm}) = e_{q+} - g_{e_{q-}}(e_{q+}, v_{\rm cm}). \quad (7)$$

The transformation of e_{q+} to e_{q_d} performed by (7) is illustrated in Fig. 15 for $v_{\rm cm} = \Delta/16$. The equivalent block diagram representation of the DCMR flash ADC implied by (7) is shown in Fig. 16.

A. Behavior of the DCMR Flash ADC Within the $\Delta\Sigma$ Modulator

It has been shown in [11] that the time average PSD of the output of the second-order ADC $\Delta\Sigma$ modulator of Fig. 1 with an ideal 33-level quantizer is that of the input signal plus white noise shaped by a $(1-z^{-1})^2$ filter provided the input has a noise component. In practice, this condition is satisfied because of the

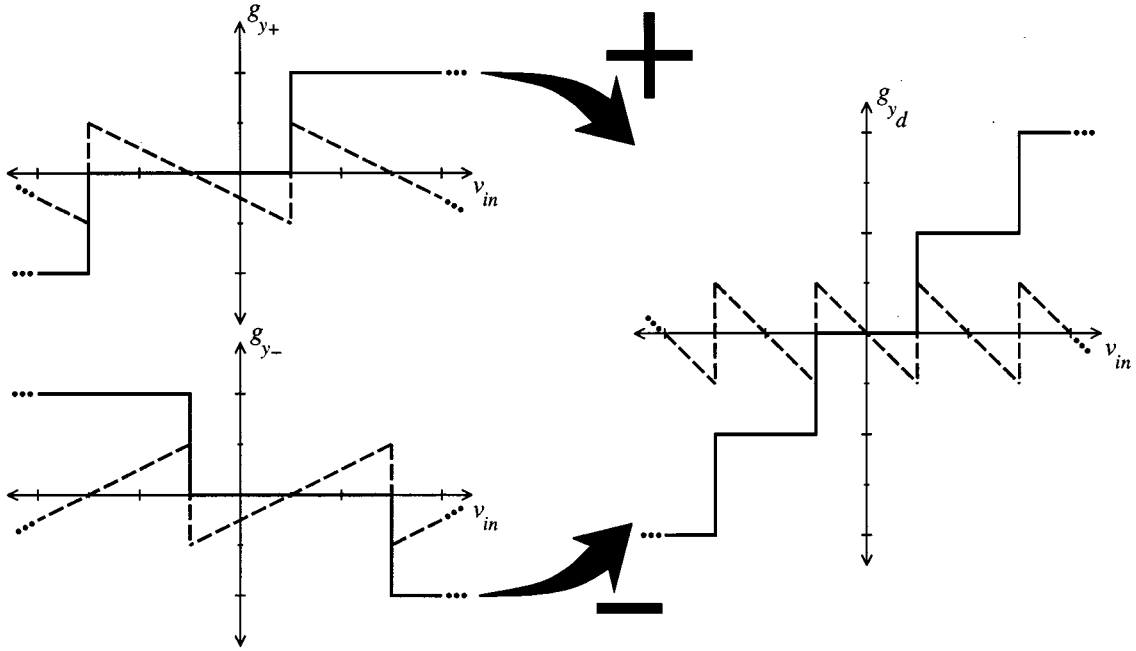

Fig. 14. DCMR flash ADC output and quantization error transfer functions with $v_{\rm cm} = \Delta/8$.

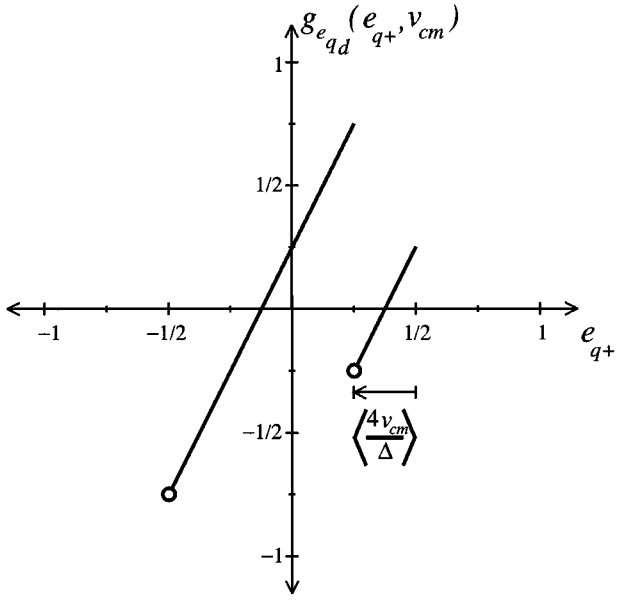

Fig. 15. The DCMR flash ADC's quantization error in terms of that of the positive flash ADC and the common-mode signal; note that $-\Delta/2 < e_{q+} \leq \Delta/2$.

inevitable thermal noise present at the input of an ADC $\Delta\Sigma$ modulator. As the $\Delta\Sigma$ modulator operates, the accumulation of the input noise within the loop filter effectively decorrelates successive values of the quantization error and decorrelates the quantization error from the input signal. Thus, as $n \to \infty$, the injected quantization error $e_q[n]$ converges to an uncorrelated sequence of random variables with a uniform probability density on $(-1/2, 1/2]$. In practice, the convergence occurs so quickly that the measured (i.e., time average) autocorrelations and PSDs of the $\Delta\Sigma$ modulator's output are indistinguishable from those that would result from white noise passed through a $(1 - z^{-1})^2$ filter.

Despite the fact that the DCMR flash ADC behaves in general as a nonuniform quantizer, the analysis is applied below to show that its quantization error is asymptotically a sequence of pairwise independent random variables with a distribution that depends on the common-mode noise. It is also shown that the presence of common-mode noise actually reduces the power of the quantization error signal.

The prototype $\Delta\Sigma$ modulator's block diagram is shown in Fig. 17(a). It can be verified that it is functionally equivalent to the block diagram of Fig. 17(b) with

$$F(z) = \frac{z^{-2}}{(1 - z^{-1})^2} \tag{8}$$

$$G(z) = -\frac{z^{-2}}{(1 - z^{-1})^2} - \frac{2z^{-1}}{(1 - z^{-1})}. \tag{9}$$

Because the impulse response of $G(z)$ takes on only integer values for all n, the feedback signal to the quantizer only changes the quantizer's input by an integer multiple of Δ, the quantization step. In [11], it is noted that when the quantizer is not overloaded, the quantization error transfer function is periodic in Δ and therefore the $G(z)$ feedback signal has no effect on the value of the quantization error.

Provided that the $\Delta\Sigma$ modulator input and common-mode noise do not overload the single-ended flash ADCs, (2), (4), and (5) imply that the DCMR flash ADC's transfer function is a periodic function of $v_{\rm in}$ with period Δ and therefore can be moved outside the feedback loop as shown in Fig. 17(c). Using (7), the DCMR flash ADC's quantization error e_{q_d} can be viewed as the quantization error of the positive flash ADC followed by a transformation of the positive ADC's quantization error according to (6). It is shown in the next section that the

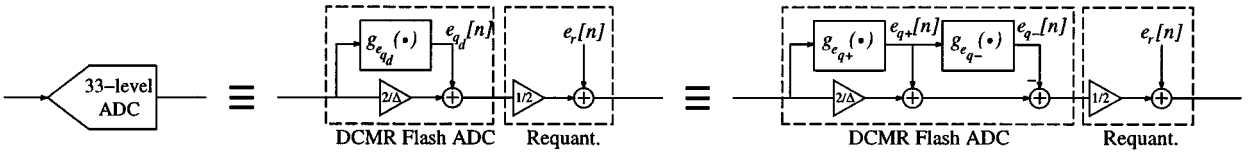

Fig. 16. Equivalent block diagram representations of the DCMR flash ADC.

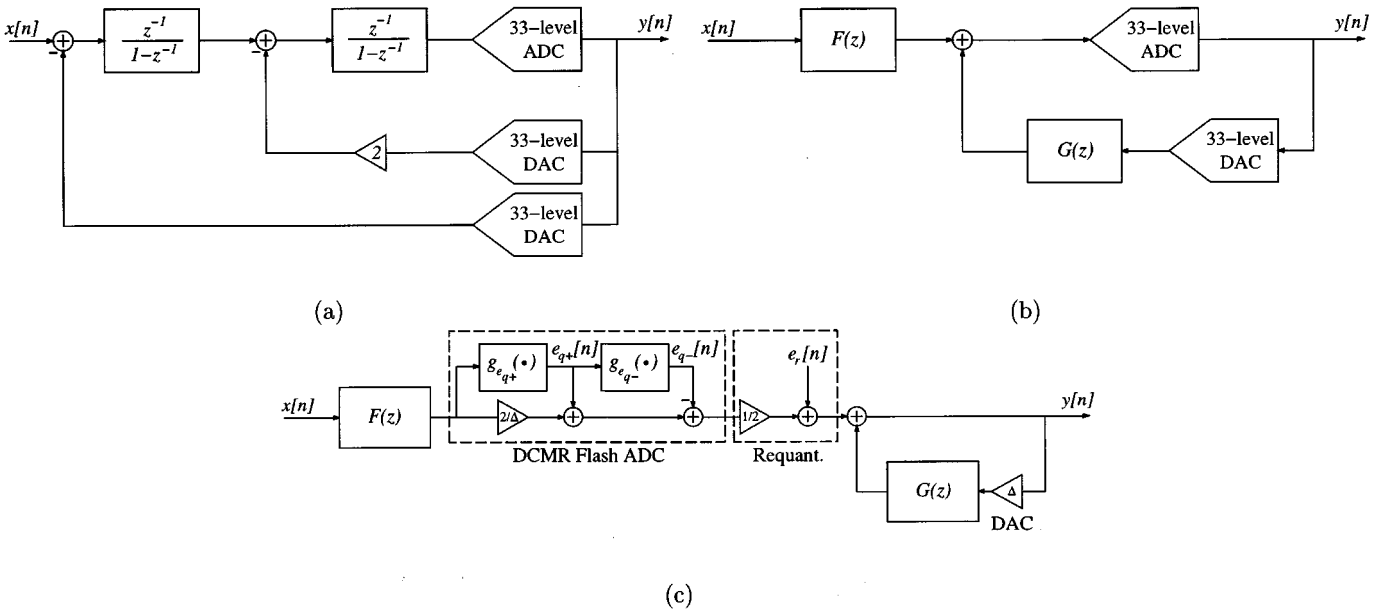

Fig. 17. Equivalent block diagram representations of the prototype $\Delta\Sigma$ modulator showing that DCMR flash ADC and requantizer can be viewed as additive noise sources outside the $G(z)$ feedback loop.

requantizer can also be moved outside the $G(z)$ feedback loop as illustrated in Fig. 17(c).

With the DCMR flash ADC removed from the $G(z)$ feedback loop, the input to the positive flash ADC is the input signal plus thermal noise passed through $F(z)$, a cascade of two discrete-time integrators. This gives rise to the decorrelation of successive samples of the quantization error mentioned earlier. Specifically, as $a \to -\infty$, where a is the time at which the $\Delta\Sigma$ modulator is started from reset, $e_{q+}[n]$ converges to a sequence of uniformly distributed random variables independent of the input signal, where $e_{q+}[n_1]$ and $e_{q+}[n_2]$ are independent for any $n_1 \neq n_2$. Details of this result are presented in Theorem 1 and Corollary 2 of the Appendix. It is also shown in Theorem 3 of the Appendix that the ensemble limits and time-average limits converge to the same value. Thus, the asymptotic behavior of the quantization error can be observed by measuring the time-average autocorrelations and PSDs.

Because $e_{q_d}[n]$ is a memoryless transformation of $e_{q+}[n]$, it follows that $e_{q_d}[n]$ is also asymptotically a pairwise independent sequence of random variables independent of the $\Delta\Sigma$ modulator's input and that $e_{q_d}[n_1]$ and $e_{q_d}[n_2]$ are asymptotically independent for $n_1 \neq n_2$. A graphical representation of the transformation of $f_{e_{q+}}(e_{q+})$ to $f_{e_{q_d}}(e_{q_d})$ by (7) is shown in Fig. 18 for $v_{\rm cm} = \Delta/16$. It follows from (6) and (7) that the probability

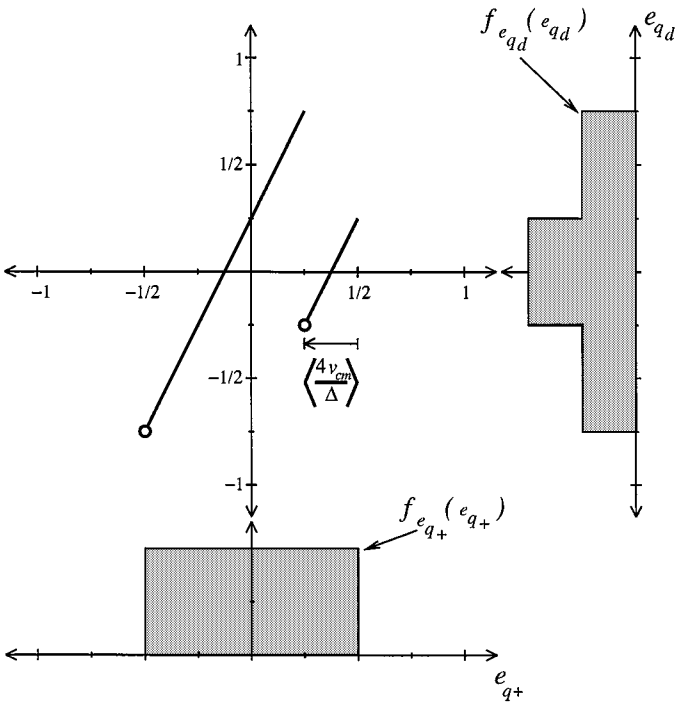

Fig. 18. A graphical representation of the transformation of $f_{e_{q+}}(e_{q+})$ to $f_{e_{q_d}}(e_{q_d})$ for $v_{\rm cm} = \Delta/16$.

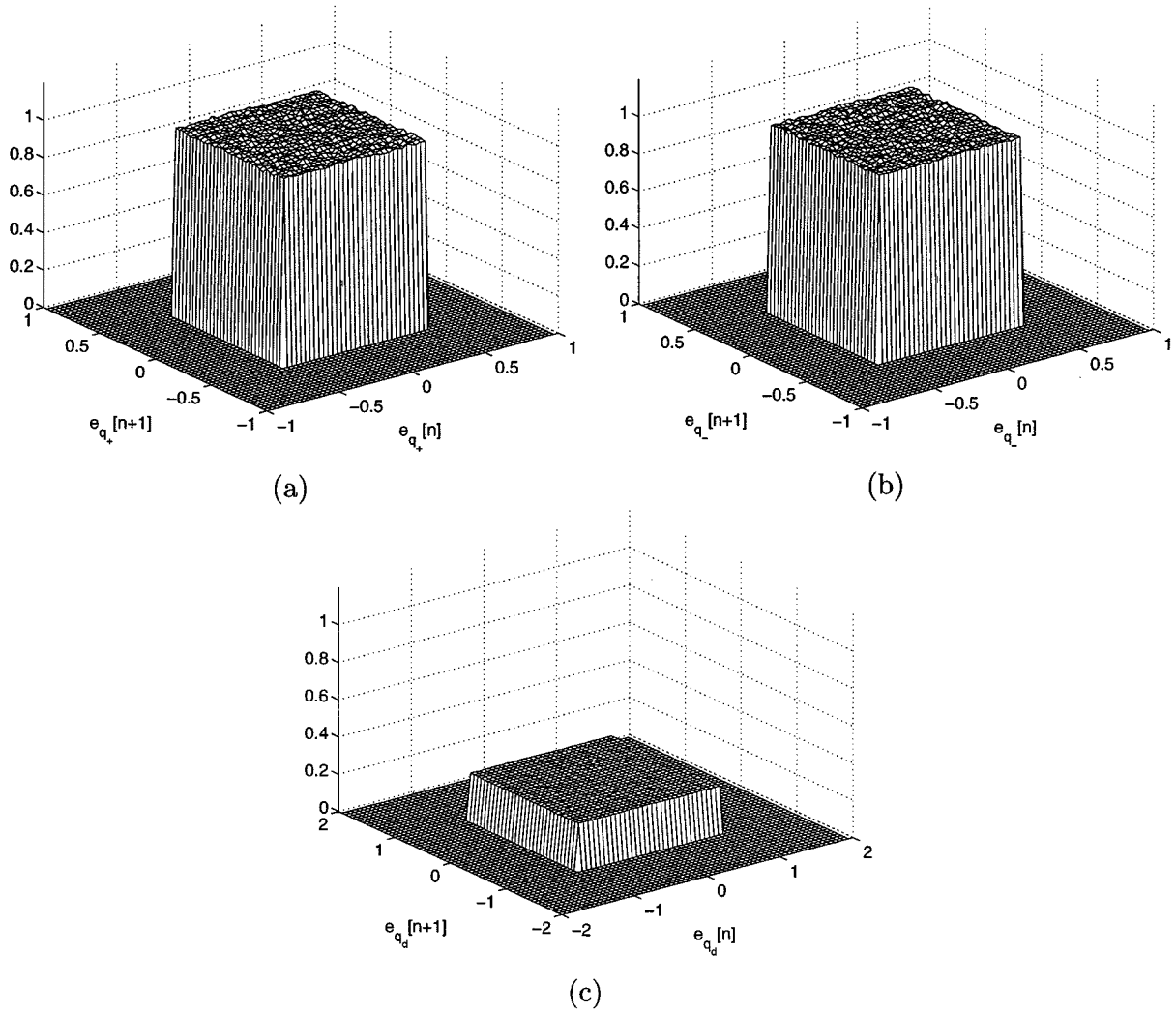

Fig. 19. Simulated probability densities for $v_{\rm cm} = 0$: (a) $(e_{q+}[n], e_{q+}[n+1])$; (b) $(e_{q-}[n], e_{q-}[n+1])$; and (c) $(e_{q_d}[n], e_{q_d}[n+1])$.

density of the DCMR flash ADC's quantization error for arbitrary values of $v_{\rm cm}$ is given by

$$f_{e_{q_d}}(e_{q_d}|v_{\rm cm}) = \begin{cases} \frac{1}{2}, & -1 + \left\langle \frac{4v_{\rm cm}}{\Delta} \right\rangle < e_{q_d} \le -\left\langle \frac{4v_{\rm cm}}{\Delta} \right\rangle \\ 1, & -\left\langle \frac{4v_{\rm cm}}{\Delta} \right\rangle < e_{q_d} \le \left\langle \frac{4v_{\rm cm}}{\Delta} \right\rangle \\ \frac{1}{2}, & \left\langle \frac{4v_{\rm cm}}{\Delta} \right\rangle < e_{q_d} \le 1 - \left\langle \frac{4v_{\rm cm}}{\Delta} \right\rangle \\ 0, & \text{otherwise.} \end{cases} \tag{10}$$

It can be verified using (10) that the power of the DCMR flash ADC's quantization error given $v_{\rm cm}$ is given by

$$E\{e_{q_d}^2|v_{\rm cm}\} = \left\langle \frac{4v_{\rm cm}}{\Delta} \right\rangle^2 - \left\langle \frac{4v_{\rm cm}}{\Delta} \right\rangle + \frac{1}{3}. \tag{11}$$

This implies that $1/12 \le E\{e_{q_d}^2\} \le 1/3$. Note that the DCMR quantizer is followed by an effective gain of 1/2 in the requantizer. Thus, the quantization error injected into the $\Delta\Sigma$ modulator loop by the DCMR quantizer is

$$\tfrac{1}{48} \le \tfrac{1}{4} \cdot E\{e_{q_d}^2\} \le \tfrac{1}{12}.$$

The maximum quantization error power occurs for $\langle 4v_{\rm cm}/\Delta \rangle = 0$, and the minimum occurs for $\langle 4v_{\rm cm}/\Delta \rangle = 1/2$.

Behavioral simulation results for the $\Delta\Sigma$ modulator of Fig. 1 support these analytical results. The $\Delta\Sigma$ modulator was run for 67 million samples, which is equivalent to 21 s of operation at a 3.072-MHz clock rate. Figs. 19–21 show simulated probability densities for $(e_{q+}[n], e_{q+}[n+1])$, $(e_{q-}[n], e_{q-}[n+1])$, and $(e_{q_d}[n], e_{q_d}[n+1])$, created by taking a histogram of the quantization errors over the entire simulation run. For all values of $v_{\rm cm}$, the distribution of $(e_{q+}[n], e_{q+}[n+1])$ is consistent with that of two independent, uniformly distributed random variables over $(-1/2, 1/2]$. This supports the analytical results that $e_{q+}[n]$ converges to a uniformly distributed random variable distributed on $(-1/2, 1/2]$ and that $e_{q+}[n]$ is independent of $e_{q+}[n+1]$. The same results hold for $(e_{q-}[n], e_{q-}[n+1])$ because the roles of

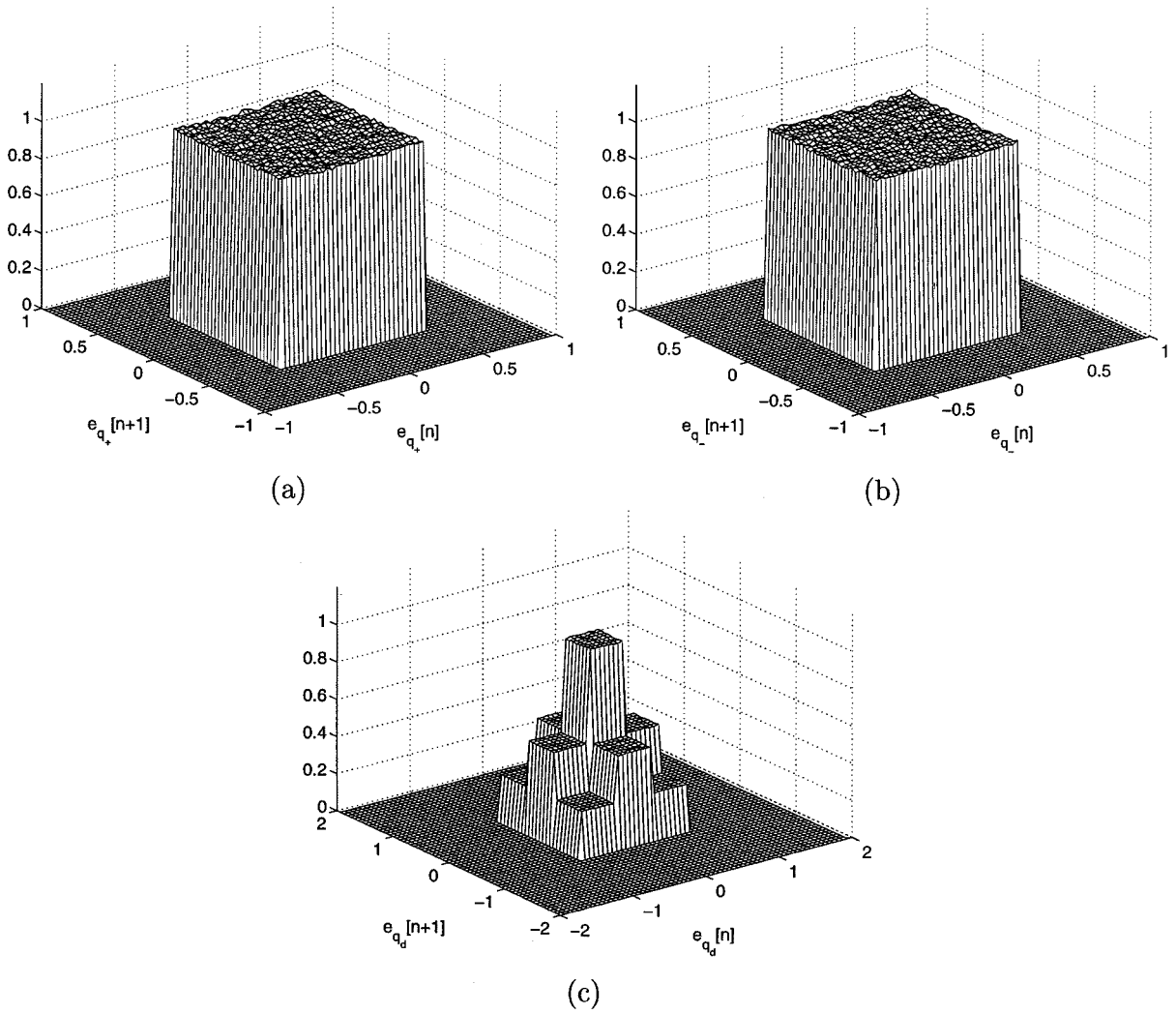

Fig. 20. Simulated probability densities for $v_{\rm cm} = \Delta/16$: (a) $(e_{q+}[n], e_{q+}[n+1])$; (b) $(e_{q-}[n], e_{q-}[n+1])$; and (c) $(e_{q_d}[n], e_{q_d}[n+1])$.

the positive and negative flash ADCs could be reversed in the preceding analysis.

Note that the simulated probability densities for $(e_{q_d}[n], e_{q_d}[n+1])$ shown in Figs. 19(c)–21(c) are consistent with those of pairs of independent random variables with marginal probability densities given by (10). For $\langle 4v_{\rm cm}/\Delta\rangle = 0$, $e_{q_d}[n]$ has a uniform distribution over $(-1, 1]$, and for $\langle 4v_{\rm cm}/\Delta\rangle = 1/2$, $e_{q_d}[n]$ has a uniform distribution over $(-1/2, 1/2]$. For $\langle 4v_{\rm cm}/\Delta\rangle = 1/4$, shown in Fig. 20(c), the joint probability density is the product of two identical distributions given by (10). These results support the analysis that shows the quantization error injected by the DCMR flash ADC at time n and $n+1$ are asymptotically independent.

B. Noise-Shaped Requantizer

As indicated by (5), the DCMR flash ADC implements a quantizer with step size Δ followed by a gain of two. Therefore, a gain of 1/2 is required to obtain an overall quantizer gain of $1/\Delta$. As seen in Fig. 12, the DCMR flash ADC takes on only even values when $v_{\rm cm} = 0$. In this case, the gain of 1/2 could be implemented by truncating the LSB. However, when common-mode noise is present, as in Fig. 13, the output takes on even and odd values, and truncation alone results in additional quantization error.

The requantization circuit shown in Fig. 6 reduces the 65-level signal $y_d[n]$ to a 33-level signal $y[n]$ by adding a signal $s[n]$ before dividing by two, where

$$s[n] = \begin{cases} \pm 1, & y_d[n] \text{ odd} \\ 0, & y_d[n] \text{ even.} \end{cases} \tag{12}$$

This implies that the error due to requantization $e_r[n]$ is

$$e_r[n] = \frac{s[n]}{2}.$$

Therefore, the power spectrum of $e_r[n]$ can be spectrally shaped through the appropriate choice of $s[n]$. By choosing the sign of $s[n]$ randomly when $y_d[n]$ is odd, the requantization error can be made to have a white power spectrum. Alternatively, the requantization error can be spectrally shaped out of the signal passband by making $s[n]$ a first-order spectrally shaped sequence obeying (12). This is a

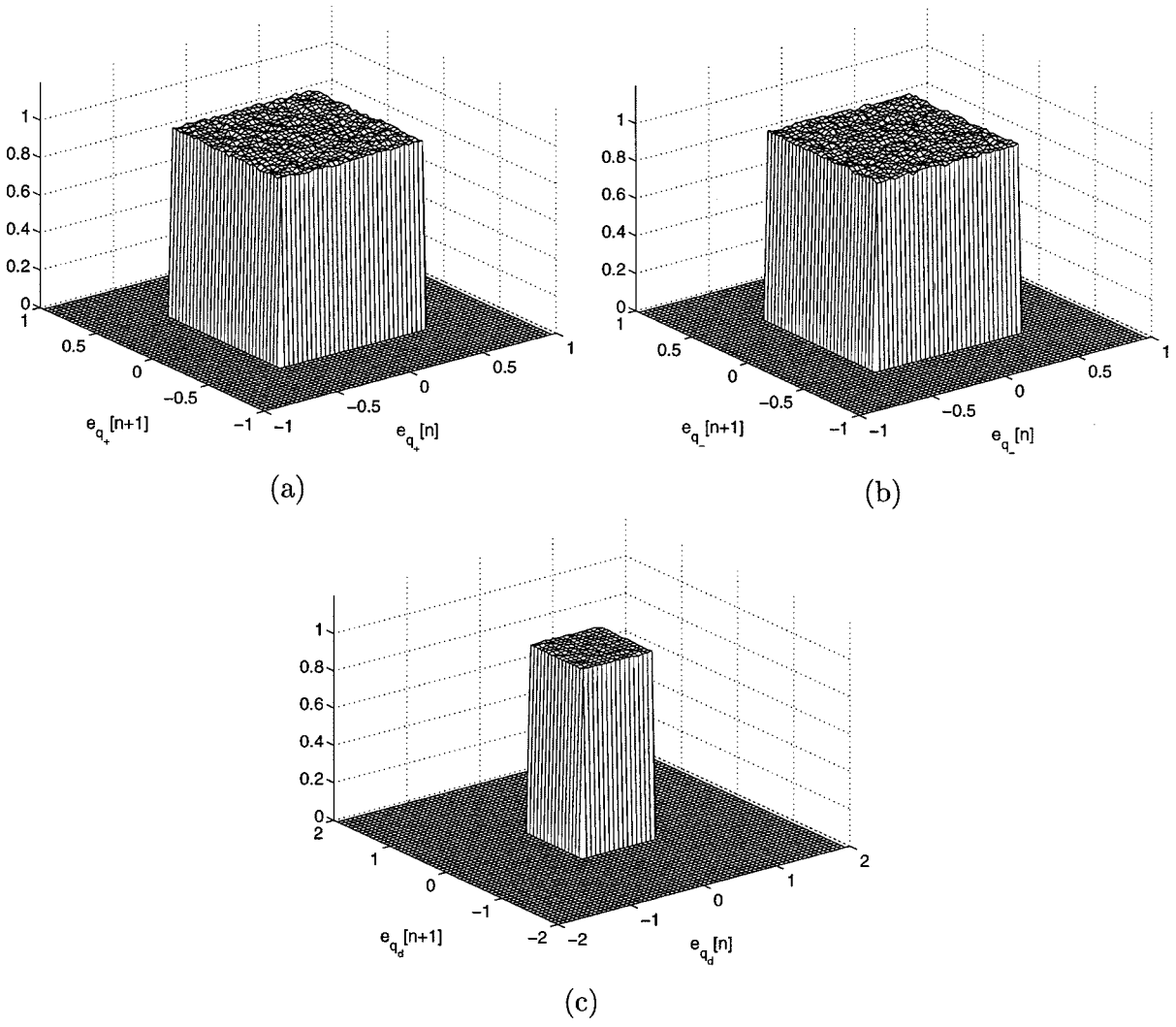

Fig. 21. Simulated probability densities for $v_{\rm cm} = \Delta/8$: (a) $(e_{q+}[n], e_{q+}[n+1])$; (b) $(e_{q-}[n], e_{q-}[n+1])$; and (c) $(e_{q_d}[n], e_{q_d}[n+1])$.

more appropriate choice in an oversampled ADC. Therefore, the dithered first-order requantizer, whose signal processing is shown in Fig. 6 and whose gate-level implementation is shown in Fig. 7, was used to generate $s[n]$. As a result, the requantization error has a first-order highpass-shaped PSD, which lies predominantly outside the signal band and is uncorrelated with the requantizer's input sequence [6].

Changing the DCMR flash ADC's input by Δ does not change the parity of the quantization error because (2) and (4) are periodic functions of $v_{\rm in}$ with period Δ. Thus, the requantizer can also be moved outside the $G(z)$ feedback loop, as shown in Fig. 17(c). Given a common-mode signal $v_{\rm cm}[n]$, the total noise power injected by the DCMR flash ADC and requantizer $e_q^2[n]$ is therefore

$$E\{e_q^2[n]\} = \tfrac{1}{4} \cdot E\{e_{q_d}^2[n]\} + E\{e_r^2[n]\}$$

where $E\{e_{q_d}^2[n]\}$ is given by (11). As indicated by the simulation results and the measured results from the $\Delta\Sigma$ modulator prototype, the combination of the DCMR flash ADC and noise-shaped requantizer provides equivalent 33-level quantization even in the presence of significant common-mode noise. The effect of the noise-shaped requantizer can be seen in the simulated and measured results, where common-mode noise is present. The slightly elevated noise power near $F_s/2$, in Figs. 8(d) and 9(b), is due to requantization of odd values at the DCMR flash ADC output.

Because (11) implies that a deliberately introduced common-mode offset can reduce the power of the quantization error by 6 dB, an interesting question is whether a pair of 33-level flash ADCs with $v_{\rm cm} = \Delta/8$ could be used to implement 65-level quantization with a 65-level feedback DAC. Without the requantizer, it seems this approach would yield a 1-bit improvement in signal-to-quantization-noise ratio.

Unfortunately, this arrangement violates one of the assumptions used to move the quantizer outside the $G(z)$ feedback loop and prove that the quantization error becomes asymptotically white. With 65-level feedback and 33-level positive and negative flash ADCs, the $G(z)$ feedback signal in Fig. 17 is no longer an integer multiple of the flash ADCs' step size. In this case, the $G(z)$ feedback signal does affect the quantization error, and the quantizers must be analyzed within the $G(z)$ feedback loop.

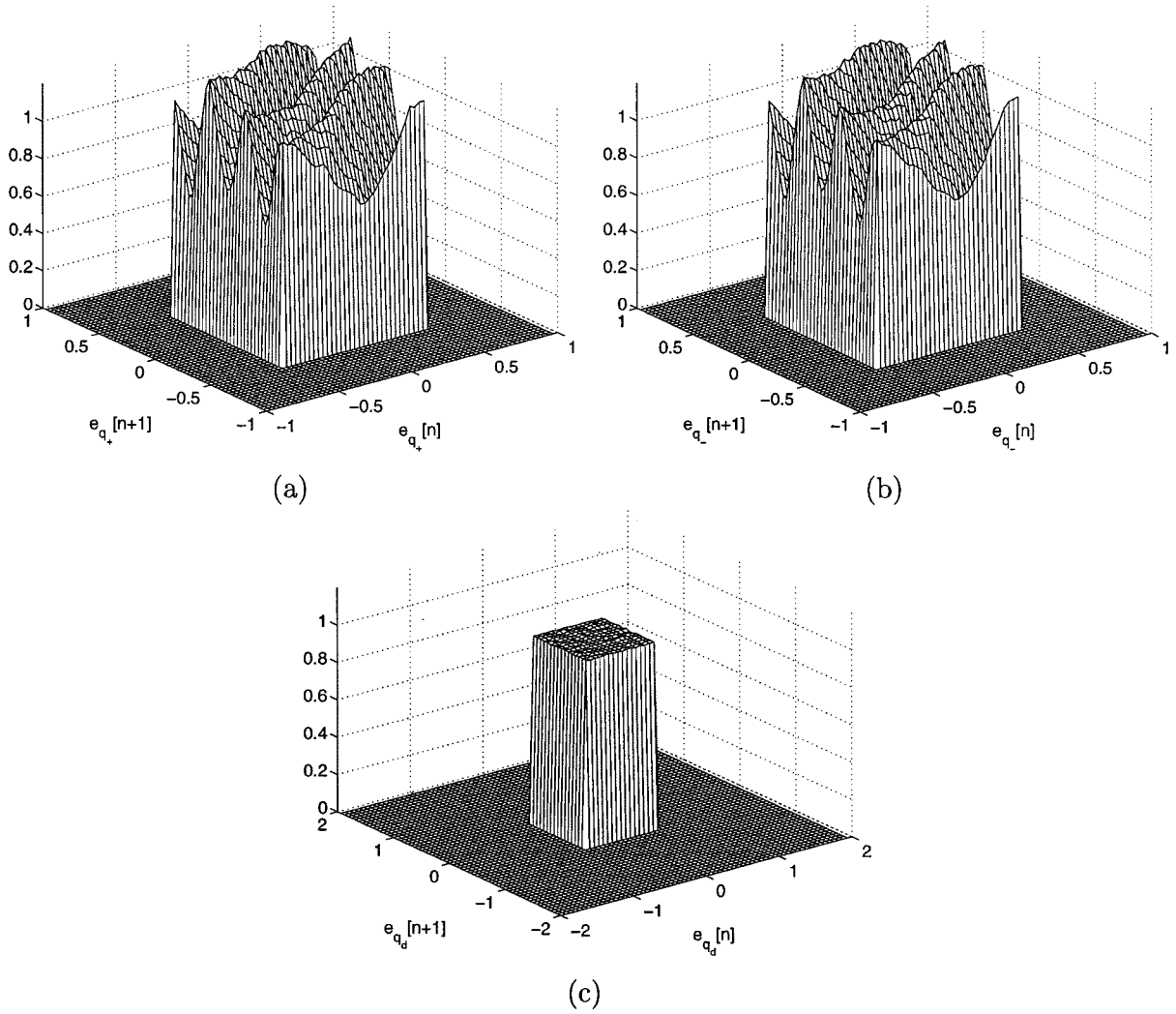

Fig. 22. Simulated probability densities with no requantizer, 65-level feedback for $v_{\rm cm} = \Delta/8$: (a) $(e_{q+}[n], e_{q+}[n+1])$; (b) $(e_{q-}[n], e_{q-}[n+1])$; and (c) $(e_{q_d}[n], e_{q_d}[n+1])$.

Simulation results shown in Fig. 22 for the $\Delta\Sigma$ modulator with 65-level feedback and no requantizer indicate that for $v_{\rm cm} = \Delta/8$, the DCMR flash ADC's quantization error is white despite the fact that the quantization error sequences of the individual flash ADCs are not white. However, as shown in Fig. 23 for $v_{\rm cm} = \Delta/16$, the surface of the joint distribution of $(e_{q_d}[n], e_{q_d}[n+1])$ has "waves" on its surface, indicating that $e_{q_d}[n+1]$ depends on the value of $e_{q_d}[n]$. This effect cancels in the distribution of $(e_{q_d}[n], e_{q_d}[n+1])$ only if $v_{\rm cm}$ is exactly $\Delta/8$. If this condition could be achieved, this technique would be useful, though common-mode offset or noise will lead to spurious tones in the $\Delta\Sigma$ modulator's output.

IV. Conclusion

A digital common-mode rejection technique with noise-shaped requantization has been presented for implementing an area-efficient differential input flash ADC and has been demonstrated in the context of a multibit ADC $\Delta\Sigma$ modulator. The use of digital common-mode rejection avoids the die area penalty and circuit design challenges of analog common-mode rejection techniques in a 3.3-V single-poly CMOS fabrication process. Simulation results and measured performance of the ADC $\Delta\Sigma$ modulator IC prototype demonstrate that the DCMR flash ADC provides high common-mode rejection and enables the $\Delta\Sigma$ modulator to achieve an SFDR of 105 dB.

Analysis of the DCMR flash ADC shows that it can be viewed as a conventional quantizer followed by an memoryless transfer function, which transforms the quantization error probability density. Previously derived results in [11] are applied to show that the quantization error is asymptotically a sequence of pairwise independent random variables and that the quantization error power is actually reduced by a nonzero common-mode voltage. Thus, the 33-level DCMR flash ADC does not introduce spurious tones in the presence of common-mode noise, and its quantization error power is less than or equal to that of a conventional 33-level flash ADC. The noise-shaped requantizer reduces the 65-level DCMR output signal to a 33-level signal and causes the requantization error to lie predominantly outside the signal band.

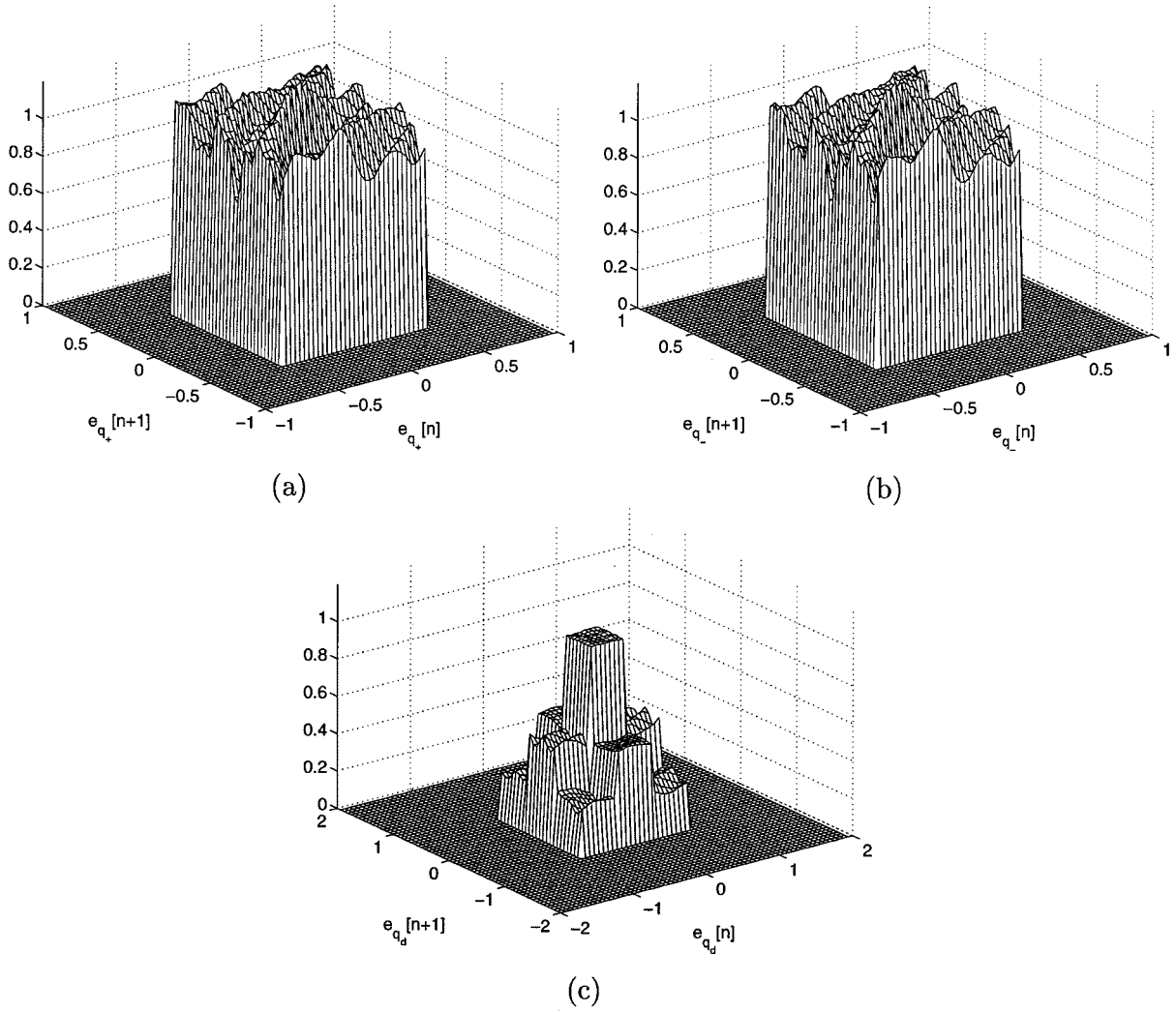

Fig. 23. Simulated probability densities with no requantizer and 65-level feedback for $v_{\rm cm} = \Delta/16$: (a) $(e_{q+}[n], e_{q+}[n+1])$; (b) $(e_{q-}[n], e_{q-}[n+1])$; and (c) $(e_{q_d}[n], e_{q_d}[n+1])$.

APPENDIX

This Appendix presents a derivation of the properties of the positive flash ADC's quantization error referenced in Section III using the theorems proven in [11]. The $\Delta\Sigma$ modulator shown in Fig. 17 is considered with $F(z)$ and $G(z)$ given by (8) and (9), respectively. Let the input to the $\Delta\Sigma$ modulator be $x[n] = x_d[n] + \eta[n]$, where $x_d[n]$ is the desired input signal and $\eta[n]$ is an i.i.d. noise sequence. The noise sequence $\eta[n]$ models the thermal noise present at the input of any practical ADC $\Delta\Sigma$ modulator. The results presented below hold no matter how low the power of the thermal noise. Let a represent the time at which the $\Delta\Sigma$ modulator is started with zero initial conditions, and let $x[n] = 0$ for $n < a$.

Claim 1: The following conditions hold for the $\Delta\Sigma$ modulator of Fig. 17 with the DCMR flash ADC and requantizer, where $F(z)$ is given by (8) and $G(z)$ is given by (9).

1) The positive flash ADC behaves as a uniform mid-step quantizer with quantization step size Δ.
2) The impulse response of $G(z)$ is integer-valued for all n.
3) The impulse response of $F(z)$ does not converge to zero as $n \to \infty$.
4) For each $p \neq 0$, the sequence $t_0 f[n] + t_1 f[n+p]$ does not converge to zero as $n \to \infty$ for any nonzero (t_0, t_1).

Proof: By design, the positive flash ADC is a uniform mid-step quantizer with step size $\Delta/2$. As shown in Fig. 17, the requantizer's gain of 1/2 cancels the gain of two in the DCMR flash ADC and makes the effective quantization gain $1/\Delta$. Thus, the positive flash ADC can be viewed as a uniform mid-step quantizer with step size Δ.

The impulse response of $G(z)$ is $g[n] = (3-n)u[n]$, where

$$u[n] = \begin{cases} 1, & n \geq 0 \\ 0, & \text{otherwise.} \end{cases}$$

Thus, $g[n]$ is integer-valued for all n.

The impulse response of $F(z)$ is $f[n] = (n-1)u[n-2]$. Thus, it does not converge to zero as $n \to \infty$. Let $z[n] = t_0 f[n] + t_1 f[n+p]$ for $p \neq 0$. For $n > \max(2, 2-p)$

$$z[n] = (t_0 + t_1)(n-1) + t_1 p.$$

Therefore, $(t_0, t_1) \neq (0, 0)$ implies that $z[n]$ does not converge to zero. ■

Theorem 1: For each pair of integers n_1, n_2, $(e_{q+}[n_1], x[n_2])$ converges in distribution to $(e'_{q+}[n_1], x[n_2])$ as $a \to -\infty$, where $e'_{q+}[n_1]$ and $x[n_2]$ are independent and $e'_{q+}[n_1]$ is uniformly distributed on $(-1/2, 1/2]$.

If $n_1 \neq n_2$ and part 4 of Claim 1 holds, then $(e_{q+}[n_1], e_{q+}[n_2])$ converges in distribution to $(e'_{q+}[n_1], e'_{q+}[n_2])$ as $a \to -\infty$, where $e'_{q+}[n_1]$ and $e'_{q+}[n_2]$ are independent.

Proof: Let $e_{q+}[n_1] = 1/2 - U_{n_1 - a}$, where

$$U_p = \left\langle \mu_p + \sum_{m=0}^{p} c_m \alpha_m \right\rangle$$
$$\mu_p = \frac{2c[p+a]}{\Delta} + \frac{1}{2} + \frac{1}{\Delta} \sum_{m=0}^{p} f[m] x_d[p+a-m]$$
$$c_m = \frac{f[m]}{\Delta}, \qquad \alpha_m = \eta[p+a-m].$$

Define

$$V_p = \left\langle \nu_p + \sum_{m=0}^{p} d_m \alpha_m \right\rangle, \qquad \nu_p = 0, \quad d_m = c_m^2.$$

By part 3) of Claim 1, $\lim_{m \to \infty} f(m) \neq 0$. This implies $\{t_0 c_m + t_1 d_m\} \not\to 0$ unless $(t_0, t_1) = (0, 0)$. Therefore, U_p and V_p satisfy the hypotheses of [11, Lemmas A1 and A2] and

$$(e_{q+}[n_1] x[n_2]) \to (\tfrac{1}{2} - U, x[n_2])$$

where U and $x[n_2]$ are independent and U is uniformly distributed on [0, 1). Therefore, $e'_{q+}[n_1] = 1/2 - U$ and is uniformly distributed on $(-1/2, 1/2]$.

To prove the second result, let $e_{q+}[n_1]$ be defined as above. Let $e_{q+}[n_2] = 1/2 - V_{n_2 - a}$, where

$$V_p = \left\langle \nu_p + \sum_{m=0}^{p} d_m \alpha_m \right\rangle$$
$$\nu_p = \frac{2c[p+a]}{\Delta} + \frac{1}{2} + \frac{1}{\Delta} \sum_{m=0}^{p} f[m] x_d[p+a-m]$$
$$d_m = \frac{f[m]}{\Delta}, \qquad \alpha[m] = \eta[p+a-m].$$

As above, $\{t_0 c_m + t_1 d_m\} \not\to 0$ unless $(t_0, t_1) = (0, 0)$. Therefore, U_p and V_p satisfy the hypotheses of Lemma A1 and

$$(e_{q+}[n_1] e_{q+}[n_2]) \to (\tfrac{1}{2} - U, \tfrac{1}{2} - V)$$

where U and V are independent. ■

Corollary 2:

$$R_{e_{q+}e_{q+}}[n, m] = \lim_{a \to -\infty} E\{e_{q+}[n] e_{q+}[n+m]\} = \tfrac{1}{12}\,\delta[m]$$
$$R_{x_d e_{q+}}[n, m] = \lim_{a \to -\infty} E\{x_d[n] e_{q+}[n+m]\} = 0.$$

The final theorem shows that the statistical averages in Corollary 2 converge to the corresponding time averages. In particular, for each m, the time averages of $e_{q+}[n]$, $e_{q+}[n] x_d[n+m]$, and $e_{q+}[n] e_{q+}[n+m]$ converge in probability to their corresponding statistical averages.

Theorem 3: As $N \to \infty$,

$$\frac{1}{N} \sum_{n=0}^{N-1} e_{q+}[n] \to 0$$
$$\frac{1}{N} \sum_{n=0}^{N-1} x_d[n] e_{q+}[n+m] \to R_{e_{q+}e_{q+}}[m].$$

If part 4 of Claim 1 holds, then

$$\frac{1}{N} \sum_{n-0}^{N-1} e_{q+}[n] e_{q+}[n+m] \to \frac{1}{12}\,\delta[m].$$

Proof: The proof is identical to that presented for Theorem 3 in [11].

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