A 12 mW ADC Delta-Sigma Modulator with 80dB of Dynamic Range Integrated in A Single-Chip Bluetooth Transceiver

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Abstract

A 12 mW switched-capacitor (*SC*) multi-bit *ADC* delta-sigma modulator for baseband demodulation integrated in a single-chip Bluetooth radio-modem transceiver achieves 77 dB of *SINAD* and 80 dB of dynamic range over a 500 kHz bandwidth with a 32 MHz sample-rate. The 1 mm^2 circuit is implemented in a 0.35 μm BiCMOS *SOI* process and operates from a 2.7 V supply.

Introduction

Manufacturers of mass market, battery-operated digital wireless transceivers such as cellular telephone handsets and wireless *LAN*s face significant market pressures, both to avoid the use of off-chip analog filters and to reduce power consumption. Direct-downconversion receivers are promising in these respects because they minimize the use of off-chip filters and allow much of the signal processing to be performed efficiently in the digital domain [1, 2, 3]. By converting the received signal band directly to dc they allow most of the channel filtering to be performed by lowpass filters which are amenable to on-chip implementation. Since analog lowpass filters with high selectivity and linearity tend to be more power hungry than comparable digital filters, a particularly efficient option is to use digital filters for the bulk of the channel filtering with analog filtering relegated primarily to anti-aliasing [1]. This approach has been proven effective in low data-rate radios such as cellular telephones, but it is more difficult in higher data-rate applications such as Bluetooth, HomeRF, and IEEE 802.11 because of the greater burden placed on the baseband *ADC*s. Nevertheless, as demonstrated by this work, low power *ADC*s with sufficient bandwidth and dynamic range for the approach to be beneficial in a Bluetooth receiver are feasible.

Specifically, the paper presents the details of a pair of low power *ADC* ΔΣ modulators for in-phase and quadrature demodulation in a single-chip Bluetooth radio-modem transceiver [4]. Each ΔΣ modulator has an input sample-rate of 32 MHz and achieves 80 dB of dynamic range over the Bluetooth baseband bandwidth of 500 kHz. The ΔΣ modulators are followed by digital comb filters which, in addition to removing out-of-band quantization noise, perform all of the required channel filtering prior to frequency detection. Each ΔΣ modulator consumes 11.9 mW of power which is significantly lower than the power consumed by other *ADC*s of similar dynamic range and bandwidth known to the authors [5, 6]. As shown in the paper, the combination of high dynamic range and low power consumption results largely from the use of a low-order ΔΣ modulator with multi-bit quantization. The multi-bit quantization is made feasible by mismatch-shaping *DAC*s modified from those presented in [7] so as to reduce processing latency.

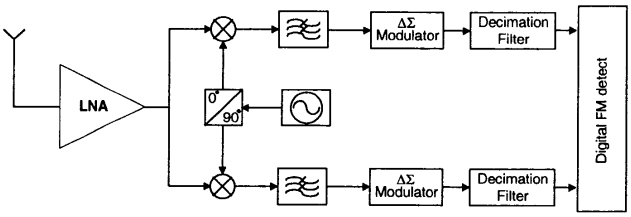

Fig. 1: Bluetooth receiver topology.

The Bluetooth Receiver Architecture

A high-level view of the Bluetooth receiver topology is shown in Fig. 1. After low noise amplification and quadrature downconversion, the in-phase and quadrature baseband signals are each passed through an anti-aliasing filter and then A/D converted by a second-order multi-bit switched-capacitor ΔΣ modulator followed by a third-order comb decimation filter. The 32 MHz sample-rate represents an oversampling ratio of 32 relative to the desired Bluetooth signal, so simple analog filters suffice for anti-aliasing purposes, and much of the overall signal processing, including channel filtering, frequency demodulation, clock and data recovery, are performed in the digital domain.

Delta-Sigma Modulator Topology

The high dynamic range and low power consumption achieved by the circuit is a result of using a low-order ΔΣ modulator with multi-bit quantization. Although a high-order single-loop architecture with one-bit quantization or a MASH architecture could have been used instead, as outlined in this Section they would have resulted in higher power consumption.

To maintain stability with one-bit quantization, the pole and zero placement in single-loop, high-order ΔΣ modulators is highly constrained. This generally results in less aggressive quantization noise shaping and a lower input no-overload

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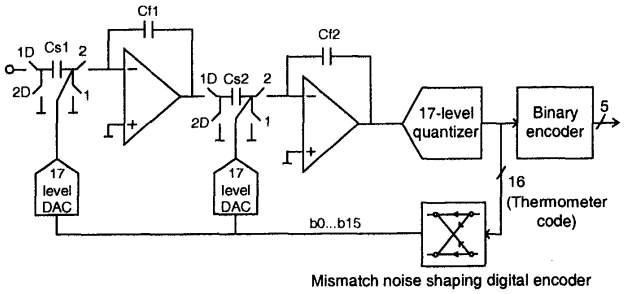

Fig. 2a: Simplified diagram of the delta-sigma modulator.

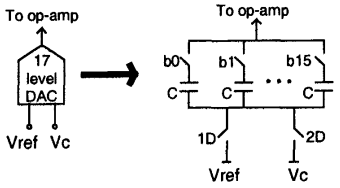

Fig. 2b: 17-level DAC.

range than is possible with multi-bit quantization. For instance, to achieve the necessary in-band dynamic range for the given frequency plan and application described in this paper, a 6th-order ΔΣ modulator would have been necessary, requiring six op-amps [8]. The lower input no-overload range generally necessitates larger input sampling capacitors to achieve a given signal to thermal noise ratio, and this gives rise to op-amp designs with greater power consumption.

MASH structures became popular for high-dynamic range applications because stable high-order ΔΣ modulators can be constructed. However, they rely on good matching between analog and digital transfer functions; in the presence of mismatches, quantization noise from the front-end stages appears at the output. This imposes constraints as to the minimum size that can be used for capacitors, and hence on the minimum power consumption that can be achieved. A popular structure consists of a 2nd-order single-loop modulator, followed by a 1st-order modulator. Although practical, the structure requires three op-amps, and the last stage op-amp sums three input signals, which increases its capacitive load, and hence its current consumption. Another limitation that results in increased power consumption is an inherent reduction of the dynamic range due to internal signal scaling.

In contrast, the multi-bit 2nd-order architecture used in the circuit presented here requires only two op-amps. Furthermore, its no-overload range is nearly equal to its reference voltage which allowed for smaller input sampling capacitors compared to the other architectures, and, hence, op-amps with lower power consumption. As described in the next Section, the architecture does require a significant amount of digital logic to implement the mismatch-shaping *DAC*s, but the power consumed by this logic was small

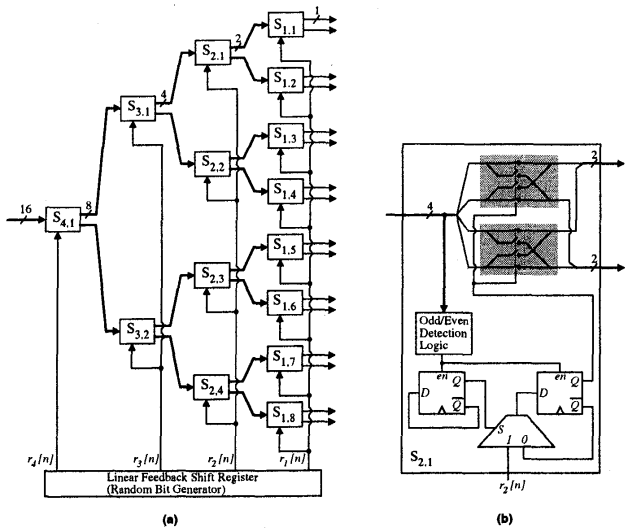

Fig. 3: (a) The tree structured mismatch shaping noise encoder consisting of 15 switching blocks. (b) The details of the (2, 1) switching block.

compared to the power consumed by the rest of the circuit.

Figure 2a shows the *SC* level topology of the ΔΣ modulator. It consists of two delaying *SC* integrators, a 17-level flash *ADC*, a mismatch-shaping digital encoder, and a pair of 17-level *DAC*s. Each 17-level *DAC* consists of 16 one-bit switched-capacitor *DAC* elements as shown in Fig. 2b.

Mismatch-Shaping Digital Encoder Details

The most efficient mismatch noise shaping digital encoder in terms of area and power consumption known to the authors is the tree-structured digital encoder presented in [7]. Therefore, the ΔΣ modulator presented in this paper uses a digital encoder based on that presented in [7]. However, modifications were necessary to facilitate higher-speed operation. Specifically, the signal processing implemented by the modified digital encoder uses thermometer encoding in place of binary-weighted encoding. This modification allows the use of transmission gates that can be configured prior to the availability of data from the flash *ADC*, thereby significantly reducing latency through the digital encoder while only slightly increasing the associated area and power consumption.

The modified digital encoder is shown in Fig. 3. It consists of *switching blocks*, labeled $S_{k,r}$ with $1 \le k \le 4$, $1 \le r \le 8$ in the figure. The numerical value associated with any given switching block input or output is taken to be ½ times the number of high bits minus ½ times the number of low bits. Thus, the digital encoder input, which consists of 16 bits, can assume values only in the range {–8, –7, ..., 8}. Each switching block generates a pair of outputs given by $(x_{k,r}[n] \pm s_{k,r}[n])/2$, where $x_{k,r}[n]$ is the switching block input, and $s_{k,r}[n]$ is a *switching sequence* generated within the switching block. If $s_{k,r}[n]$ is such that the switching block outputs are in the set

$\{-2^{k-2}, -2^{k-2}+1, \ldots, 2^{k-2}\}$ then the switching block is said to satisfy the *number conservation rule*. As shown in [9], provided the number conservation rule is satisfied by all the switching blocks, the DAC mismatch noise is a linear combination of the switching sequences with coefficients that depend only on the capacitor mismatches (which are assumed to be time-invariant). Thus, to cause the mismatch noise to have a specific spectral property (e.g., to be first-order shaped noise), all the switching sequences must be chosen to satisfy the number conservation rule *and* have the desired spectral property.

It can be verified that the $S_{2,1}$ switching block shown in Fig. 3b satisfies the above requirements and has a switching sequence with a first-order highpass power spectral density (*PSD*). It consists of two two-bit *swapper cells*, two *D* flip-flops, a 2-1 multiplexer, and logic that detects whether the input value is even or odd. Each swapper cell either passes its two input bits directly to its two outputs or interchanges their order depending upon the output of the right-most flip-flop. The pseudo-random bit from the linear feedback shift register ensures that the switching sequence does not contain spurious tones [9]. The other switching blocks with k=2 are identical to that shown in Fig. 3b, and the remaining switching blocks differ only in the number of swapper cells they contain.

Circuit Implementation Details

The same op-amp (Fig. 4) was used in both *SC* integrators in the ΔΣ modulator. *PNP* devices with large beta were not available in this process, which made the 2-stage Miller compensated amplifier a preferred candidate for low current consumption and small area. PMOS devices were used at the input for low $1/f$ noise, and NPN devices were used as the driver devices in the 2nd-stage. A conventional *SC* common-mode feedback circuit with an inverting stage was used. Over temperature, supply, loading, and process corners, the critical first-stage op-amp's simulated (in both sampling and integration phases) differential gain, unity-gain bandwidth, and phase margin were, 80 dB, 350 MHz, and 80°, respectively.

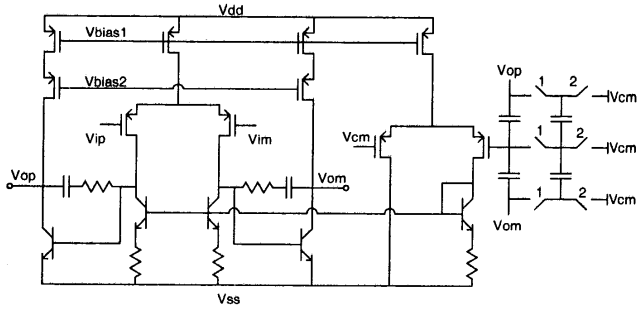

Fig. 4: Op-amp schematic.

The comparator cell used in the flash *ADC* employed NPN bipolar transistors at the input, resulting in low current consumption as well as extremely relaxed input-referred offset requirements.

To further reduce latency in the ΔΣ modulator feedback path, the flash *ADC* comparators were implemented without set-reset latches following their track-and-latch stages. Instead, set-reset latches were placed at the output lines of the digital encoder and at the output lines of the delta-sigma modulator as shown in Fig. 5. Simulations over process and temperature indicate that the worst-case latency is less than 3 nS.

The swapper cells are implemented as *CMOS* transmission gates. The timing is such that the output of the right-most flip-flop settles to the correct value prior to the time at which the data is available at the output of the flash *ADC*. Thus, the delay through the digital encoder is determined mainly by the *RC* time constants resulting from the on-resistance and stray capacitances associated with the switches. Since there are four layers (columns) of switching blocks in the digital encoder, it follows that the each input bit passes through four transmission gates before it reaches the output of the digital encoder.

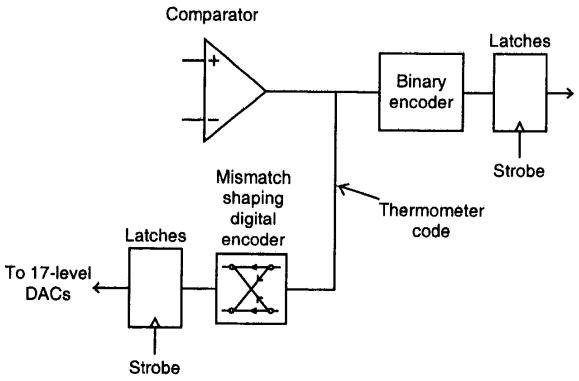

Fig. 5: Placement of the latches in the signal flow.

Experimental Results

The Bluetooth transceiver IC is implemented in a 0.35 μm SOI BiCMOS process and operates from a 2.7 V power supply. The complete ΔΣ modulator including the analog portion, the digital portion, and all supporting circuitry had a measured current consumption of 4.4 mA at a supply voltage of 2.7 V. The reference voltage is 1.4 $V_{pp,diff}$. It should be mentioned that the SOI feature of this process did not play a relevant role in reducing the power consumption, as it uses a buried epi layer, and hence significant parasitic capacitances do exist.

Measured data that indicate the performance of the ΔΣ modulator are shown in Fig. 6. A representative *PSD* for a –0.66 dBV (1.36 $V_{p,diff}$), 31.25 kHz input sinusoid is shown in Fig. 6a, and a plot of the measured *SINAD* as a function of the amplitude of a 31.25 kHz input sinusoid is shown in Fig. 6b (no appreciable differences are observed for higher values of the signal frequency). The measured peak *SINAD* is 77 dB, and the dynamic range is 80 dB. For this input signal amplitude, –0.66 dBV, the *SFDR* is 78 dB. With the mismatch-shaping logic disabled, the peak *SINAD* reduces to 62 dB. The ΔΣ modulator performance is summarized in Table 1, and a die photograph of the ΔΣ modulator portion of the Bluetooth transceiver *IC* is shown in Fig. 7.

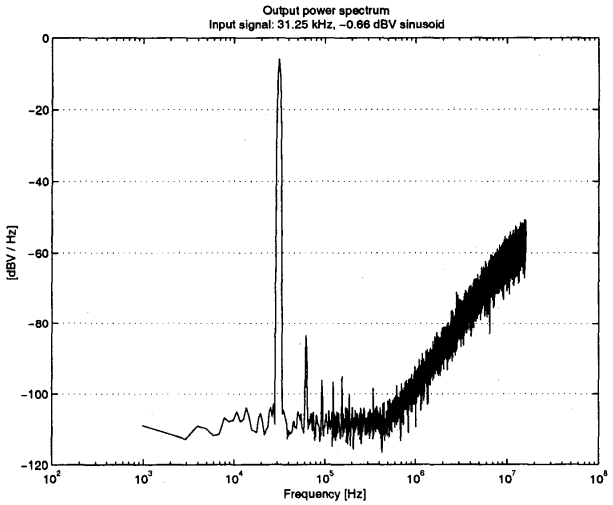

Fig. 6a: Output power spectral density, for a 1.36 $V_{p,diff}$ 31.25 kHz input sinusoid.

Table 1: Measured *ADC* performance.

Signal band	0 – 500 kHz
Sampling frequency	32 MHz
Dynamic range	80 dB
Peak SINAD	77 dB
Peak SFDR	78 dB
Power supply voltage	2.7 V
Power supply current	4.4 mA
Die Area	1.0 mm^2

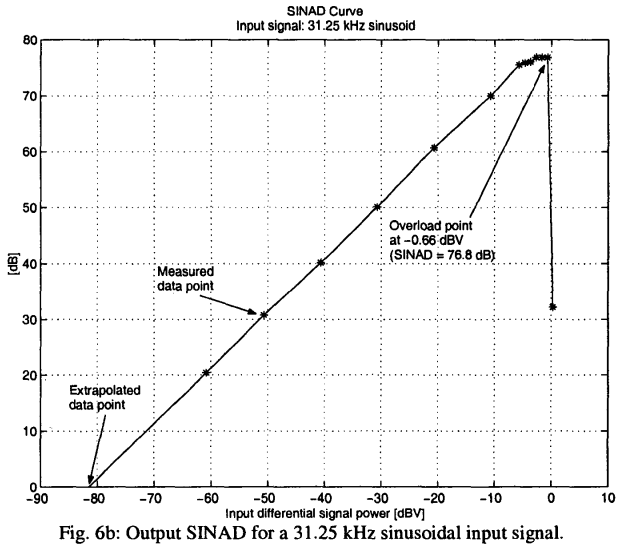

Fig. 6b: Output SINAD for a 31.25 kHz sinusoidal input signal.

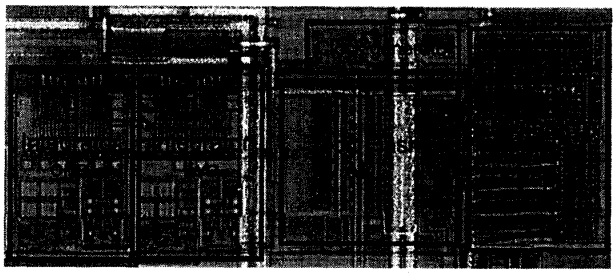

Fig. 7: Die photo of the ΔΣ modulator.

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