A 3.3-V Single-Poly CMOS Audio ADC Delta–Sigma Modulator with 98-dB Peak SINAD and 105-dB Peak SFDR

Eric Fogleman, *Student Member, IEEE*, Ian Galton, *Member, IEEE*, William Huff, *Student Member, IEEE*, and Henrik Jensen, *Member, IEEE*

***Abstract*—This paper presents a second-order $\Delta\Sigma$ modulator for audio-band analog-to-digital conversion implemented in a 3.3-V, 0.5-μm, single-poly CMOS process using metal–metal capacitors that achieves 98-dB peak signal-to-noise-and-distortion ratio and 105-dB peak spurious-free dynamic range. The design uses a low-complexity, first-order mismatch-shaping 33-level digital-to-analog converter and a 33-level flash analog-to-digital converter with digital common-mode rejection and dynamic element matching of comparator offsets. These signal-processing innovations, combined with established circuit techniques, enable state-of-the-art performance in CMOS technology optimized for digital circuits.**

***Index Terms*—analog-to-digital conversion, delta–sigma modulation, digital-to-analog conversion, dynamic element matching, linear feedback shift registers, multibit delta–sigma modulation, switched-capacitor circuits.**

I. Introduction

FOR mixed-signal IC's with high digital circuit content, single-poly CMOS optimized for digital circuits can provide the lowest overall implementation cost. For example, it is preferable to avoid the expense of double-poly capacitors, thick-oxide transistors for 5-V operation, or other analog process enhancements when analog circuits such as data converters make up only a small portion of the total die area. This is often true even if the lack of analog enhancements significantly increases the area of the analog circuitry. However, the performance that can be achieved by data converters in a digital-optimized, single-poly CMOS process may limit the extent to which this advantage can be exploited.

High-resolution data converters require linear capacitors and low-noise, low-distortion amplifier circuits to implement fundamental building blocks such as sample-and-holds, integrators, and comparators. Though the specific circuits and performance specifications are determined by the data-converter's architecture, the lack of linear capacitors with low parasitic capacitance and process-related supply-voltage restrictions in modern, digital-optimized, single-poly CMOS processes generally present key challenges in realizing high-performance data converters.

In a CMOS process without double-poly capacitors or other thin-oxide, linear capacitor structures, the metal interconnect layers or MOS structures must be used to implement capacitors. MOS capacitor structures (MOSCAP's) require special biasing to keep them in an accumulated or depleted operating region and to mitigate their inherent nonlinearity. Metal interconnect (metal–metal) capacitors are inherently linear, but for a given value of capacitance, a metal–metal capacitor can require as much as 30 times the area of a double-poly capacitor. Moreover, the bottom plate capacitance of a metal–metal capacitor is comparable to the interplate capacitance, while the double-poly capacitor's parasitic capacitance is typically less than 50% of the interplate capacitance.

Process-related limitations on supply voltages to 3.3 V or below restrict signal swings in amplifiers and through analog switches. In switched-capacitor circuits, this necessitates increased sampling capacitances to achieve the target signal-to-thermal-noise ratio. In switched-capacitor integrators, large feedback capacitances may be required to scale the output down to fit within the amplifier's output swing. Thus, the reduced headroom and increased loading complicate the task of realizing fast-settling, low-distortion, switched-capacitor circuits.

It might be possible to mitigate these problems through critical refinement of the analog circuits, but a strategy that uses digital processing to minimize the performance requirements of the analog circuits makes better use of the strengths of a digital-optimized CMOS process. Multibit $\Delta\Sigma$ modulation using mismatch-shaping digital-to-analog converters (DAC's) exemplifies this approach. By reducing the quantization noise power to be shaped out of band relative to two-level quantization, a multibit $\Delta\Sigma$ modulator can achieve the same signal-to-noise-and-distortion (SINAD) ratio with a lower order $\Delta\Sigma$ modulator and a lower oversampling ratio than a single-bit design. The reduction in $\Delta\Sigma$ modulator order implies that fewer switched-capacitor stages are required, and the reduced oversampling ratio relaxes the bandwidth and slew-rate requirements on the integrators. The mismatch-shaping DAC in the feedback path causes static DAC mismatch errors to fall predominantly outside the signal band and significantly relaxes the matching requirements on the DAC's analog components [1]–[12].

Manuscript received July 16, 1999; revised October 18, 1999. This work was supported by the National Science Foundation under Grant MIP-9711331.

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Publisher Item Identifier S 0018-9200(00)00594-1.

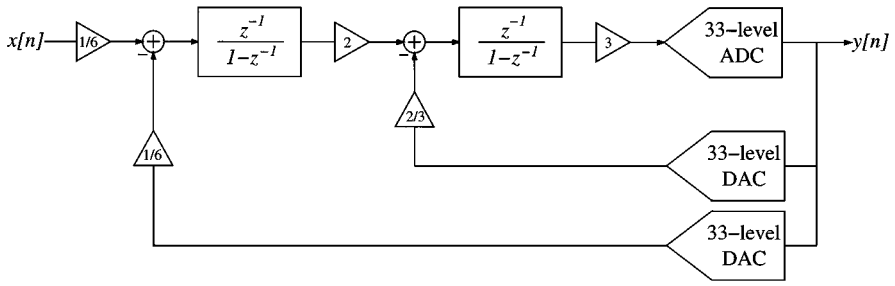


Fig. 1. The high-level $\Delta\Sigma$ modulator topology.

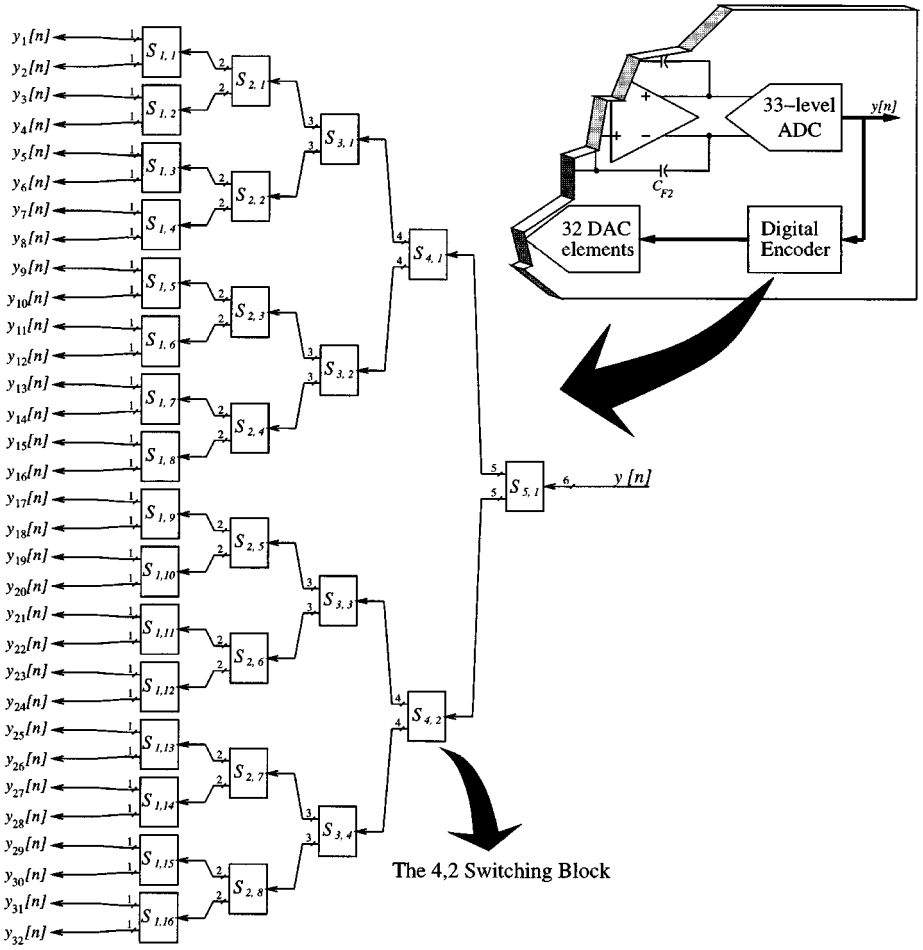


Fig. 2. Mismatch-shaping DAC encoder.

The multibit approach eases the design requirements on the switched-capacitor circuits, but it also introduces several new design challenges. The transfer function from the first integrator input to the $\Delta\Sigma$ modulator output provides no noise shaping. Therefore, the first-stage feedback DAC must have the same signal-band precision as the overall data converter. Furthermore, the reduced $\Delta\Sigma$ modulator order and oversampling ratio imply that the noise transfer function provides less attenuation of circuit noise and distortion in the flash analog-to-digital converter (ADC) quantizer. Thus the flash ADC must provide sufficient common-mode noise rejection and spurious-free dynamic range (SFDR) performance to meet the overall data-converter's performance targets.

This paper presents an audio ADC $\Delta\Sigma$ modulator implemented in a 3.3-V, 0.5-μ CMOS process using metal–metal capacitors that achieves 98-dB SINAD and 105-dB SFDR [13]. To the knowledge of the authors, this level of performance has not been achieved previously under these process constraints [14]–[16]. The $\Delta\Sigma$ modulator makes extensive use of digital processing to simplify or avoid analog circuit design problems and minimize the use of large-area metal–metal capacitors. A low-complexity mismatch-shaping DAC digital encoder provides spur-free, first-order shaping of static mismatches in the feedback DAC. The differential input flash ADC uses a pair of single-ended, 33-level flash ADCs whose binary outputs are subtracted to reject common-mode noise. The flash ADC

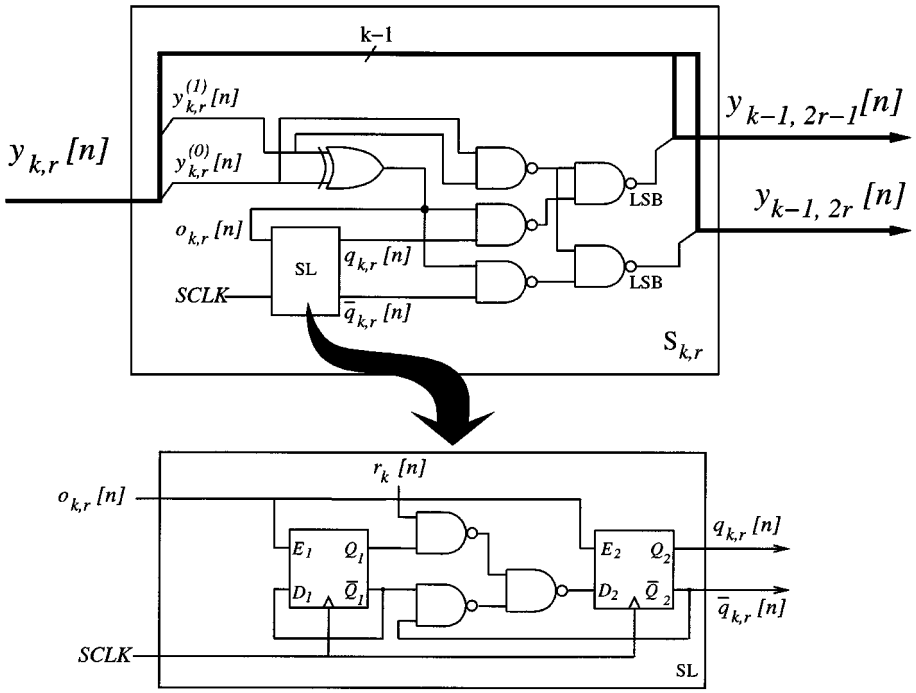


Fig. 3. Switching block implementation.

comparators use a dynamic element-matching technique to spectrally whiten spurious tones caused by their static input offsets. A modified linear feedback shift register (LFSR) efficiently provides the multiple uncorrelated pseudorandom sequences required by the mismatch-shaping DAC and flash ADC.

The remainder of this paper consists of three main sections. Section II presents the signal-processing innovations of the $\Delta\Sigma$ modulator, the mismatch-shaping DAC, the flash ADC, and the pseudorandom sequence generator. Section III provides circuit implementation details. Section IV describes the layout floorplan and presents measured performance of the $\Delta\Sigma$ modulator prototype.

II. Signal-Processing Details

A. Delta–Sigma Modulator

The prototype is based on the second-order $\Delta\Sigma$ modulator implemented with two delaying integrators presented in [17]. The $\Delta\Sigma$ modulator incorporates 33-level quantization, and the coefficients have been modified as shown in Fig. 1 to match each integrator's full-scale output to the amplifier's output swing. It operates at an oversampling ratio of 64 with an input sample rate of 3.072 MHz. In the absence of nonideal analog circuit behavior, the $\Delta\Sigma$ modulator achieves a peak signal-to-quantization-noise ratio of 108 dB over the 24-kHz signal band.

B. Mismatch-Shaping DAC Digital Encoder

The $\Delta\Sigma$ modulator uses the tree-structured mismatch-shaping DAC digital encoder presented in [11]. The encoder, shown in Fig. 2, operates on the 33-level output of the flash ADC and generates 32 single-bit select lines controlling the two banks of 32 one-bit DAC elements. The 31 switching blocks within the encoder implement a first-order mismatch-shaping algorithm.

To minimize the complexity of the encoder, the implementation shown in Fig. 3 was used to realize the 31 switching blocks [18]. This circuit is logically equivalent to the dithered first-order switching block shown in [11] but eliminates the need for adders in each block by representing the (2^b+1)-level data as b binary bits plus an additional least significant bit (LSB)-weighted bit. The resulting 33-level encoder is composed of 279 combinational logic gates and 62 D-flip-flops.

To eliminate spurious tones in the shaped DAC noise, five uncorrelated single-bit random sequences, denoted as $r_k[n], k = 1, \ldots, 5$ in Fig. 3, are used to dither the switching blocks in each layer of the encoder [18]. The use of one random sequence per layer of the digital encoder is sufficient to decorrelate the sequences generated by the 31 switching blocks. Assuming $3\sigma = 1\%$ Gaussian-distributed DAC element mismatch, the first-order encoder provides 104 dB peak SINAD.

C. Differential Flash ADC

To preserve the common-mode noise rejection benefits of the fully differential switched-capacitor circuitry, the flash ADC must quantize the second integrator's differential output with respect to a set of differential reference levels. The second-order noise transfer function provides only 52 dB of attenuation at the passband edge, and thus the flash ADC's common-mode rejection is a critical factor in meeting the $\Delta\Sigma$ modulator's 105-dB SFDR target.

A common approach to implementing a differential input flash ADC in a $\Delta\Sigma$ modulator uses a pair of switched capacitors to sample and compare the differential signal and reference levels on alternate clock phases [19], [20]. For the prototype, sampling capacitors larger than 100 fF would have been required to reduce

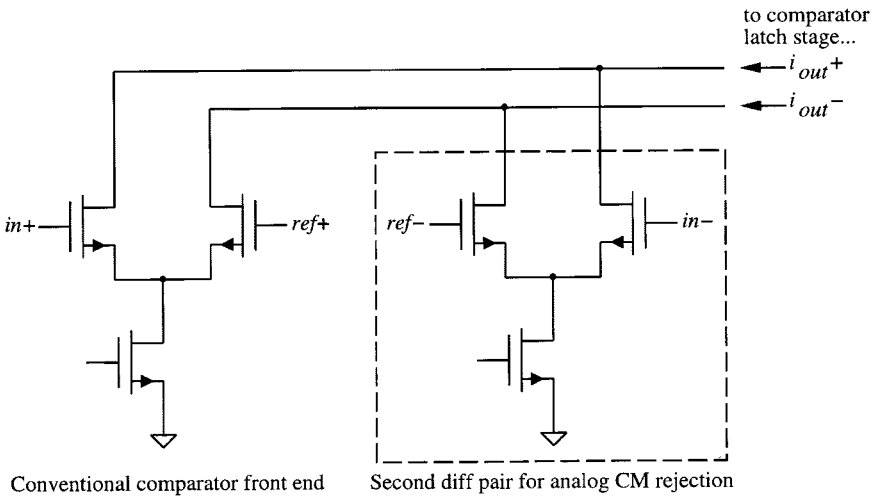


Fig. 4. A possible analog common-mode rejection technique for implementing a differential input flash ADC.

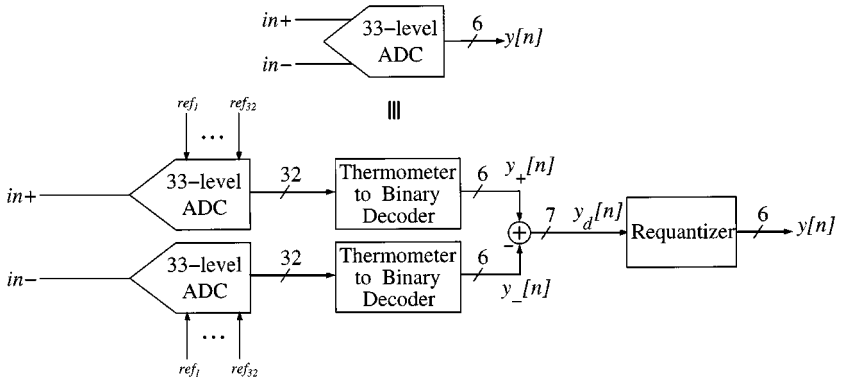


Fig. 5. High-level view of the 33-level DCMR flash ADC.

sufficiently the error caused by charge sharing with each comparator's parasitic input capacitance. If implemented this way, the 33-level flash ADC would have required an array of 64 capacitors, which would have consumed approximately 5% of the entire chip's die area. Moreover, the approach would have required a low output impedance reference ladder capable of driving switched-capacitor loads and would have contributed significant loading of the second integrator. Buffering the reference ladder with source-followers would have presented a circuit design challenge given the limited headroom, and using a low resistance ladder would have significantly increased the power dissipation. To avoid these problems, an approach that eliminates the need for switched capacitors is desirable.

In principle, an analog approach that would avoid the need for capacitors involves the use of a comparator with two differential inputs to cancel the common-mode component. Such a scheme is shown in Fig. 4, wherein the comparator converts the signals $(\text{in}_+ - \text{ref}_+)$ and $(\text{in}_- - \text{ref}_-)$ to currents using two differential pairs, subtracts the differential currents to cancel the common-mode component, and sends the resulting signal to a conventional latching stage. While this technique provides small-signal common-mode rejection, it can be verified that the common-mode signal modulates the differential transconductance. This leads to signal-dependent offsets and creates a mechanism for intermodulation of the differential and common-mode signals. Though this problem could possibly be mitigated by careful design, the approach was not used because of the aggressive $\Delta\Sigma$ modulator SFDR target.

To provide both large- and small-signal common-mode rejection without switched capacitors, the prototype incorporates digital common-mode rejection (DCMR) implemented using a pair of single-ended, 33-level flash ADCs and digital processing to cancel the common-mode noise component [21]. As shown in Fig. 5, the single-ended flash ADC outputs, $y_+[n]$ and $y_-[n]$, are subtracted to cancel the common-mode component yielding a 65-level difference signal $y_d[n]$. The difference is requantized to a 33-level signal $y[n]$ to avoid the need for a 65-level DAC.

In the absence of common-mode noise, the DCMR flash ADC is equivalent to a conventional 33-level flash ADC. In this case, the outputs $y_+[n]$ and $y_-[n]$ are complementary signals, and the difference signal $y_d[n]$ takes on only even values. Thus, dropping the LSB of $y_d[n]$ would yield the correct 33-level output.

When common-mode noise is present at the input of the DCMR flash ADC, it can be shown that the digital subtraction cancels the common-mode noise without generating spurious tones and that the quantization noise power of $y_d[n]$ is between that of a 33-level quantizer and that of a 65-level quantizer. However, $y_+[n]$ and $y_-[n]$ are not complementary in this case, so $y_d[n]$ is a 65-level signal that takes on both even and odd values. Rather than implementing a 65-level mismatch-shaping DAC digital encoder and

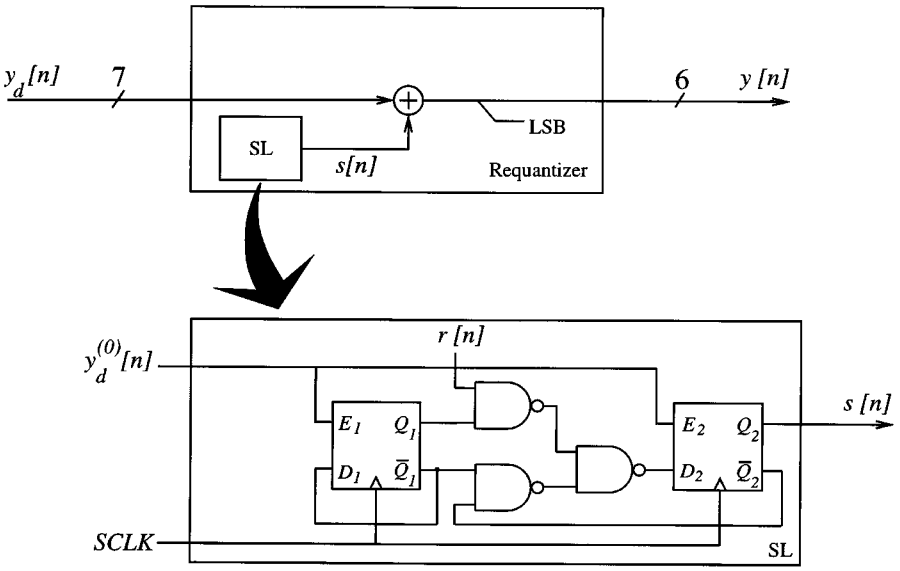


Fig. 6. Requantizer implementation.

incurring the additional hardware overhead, a noise-shaping requantizer was used to requantize $y_d[n]$ to a 33-level signal. By rounding odd values of $y_d[n]$ up or down in a first-order, noise-shaped fashion and eliminating the LSB, the circuit shown in Fig. 6 causes the requantization error to be spur-free and to fall predominantly outside the signal band [21].

Relative to a single differential input ADC, the DCMR architecture requires two single-ended, 33-level flash ADCs, a second bubble correction circuit and thermometer-to-binary encoder, a 6-bit subtractor, a 5-bit adder, a switching block of the type used in the DAC digital encoder, and a single-bit random sequence. The digital circuitry consists of 240 combinational logic gates and two D-flip-flops. As shown in Section IV, this approach yielded net area savings over the switched-capacitor implementation.

D. Dynamic Element Matching Comparator

The reduced $\Delta\Sigma$ modulator order and oversampling ratio imply that the noise transfer function provides less attenuation of distortion introduced at the quantizer, so the nonlinearity of the flash ADC can limit the SINAD and SFDR performance of the $\Delta\Sigma$ modulator. While both reference ladder resistor mismatches and comparator input offsets contribute to errors in the placement of the quantization levels, the comparator offsets are the dominant error source. Input offsets with $\sigma_{V_{os}} \approx 10$ mV are typical with the small geometry devices used in the comparators, and the resulting errors in the quantization levels are comparable to the 31.25-mV LSB of the flash ADC. Behavioral simulations confirmed that $\sigma_{V_{os}} = 10$ mV comparator offset errors could limit the SFDR performance of the $\Delta\Sigma$ modulator to below 105 dB. In contrast, 1% resistor mismatches in the reference ladder give rise to quantization-level errors on the order of 1 mV. The dominant effect of the comparator offset errors becomes even more pronounced as the number of quantization levels is increased or as the signal swings are reduced. This occurs because the offset errors are fixed and do not scale with the reference voltages as do the errors due to resistor mismatch.

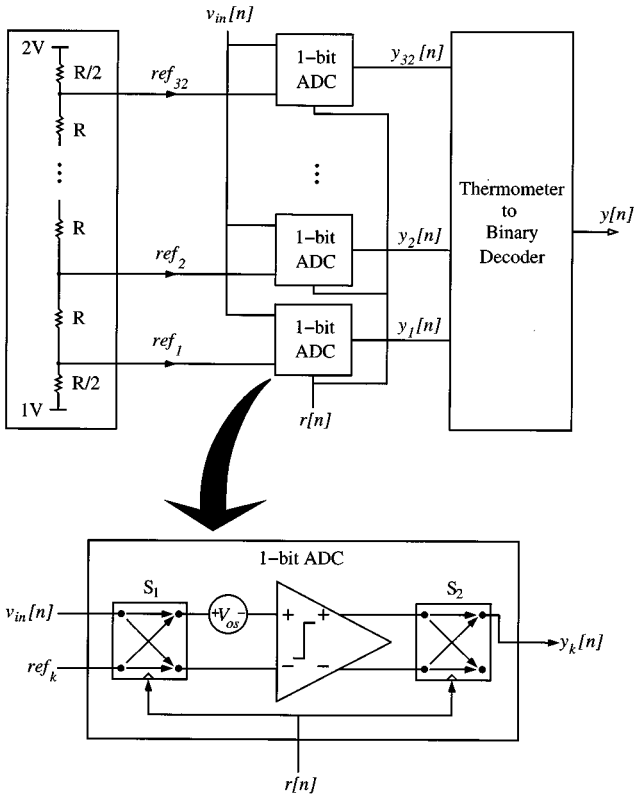


Fig. 7. Comparator offset DEM implementation.

Switched-capacitor offset calibration was not used to overcome this problem because the large-area metal–metal capacitors required for each of the 64 comparators would significantly increase the size of the flash ADC. Instead, a randomization technique was used to spectrally whiten errors caused by comparator input offsets [22]. This approach is referred to as comparator offset dynamic element matching (DEM) because of its similarity to DEM techniques used in DAC's.

Fig. 7 shows one of the single-ended flash ADCs with comparator offset DEM. The input and output of each comparator

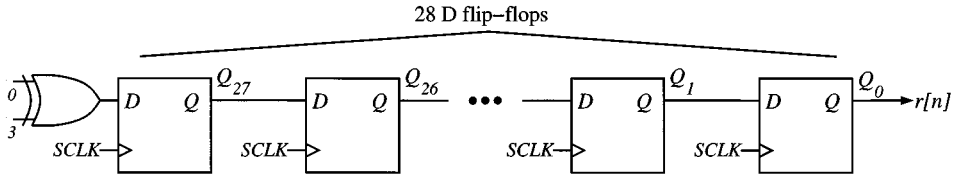


Fig. 8. A "type-I" LFSR implementing the generator polynomial $1 + x^3 + x^{28}$.

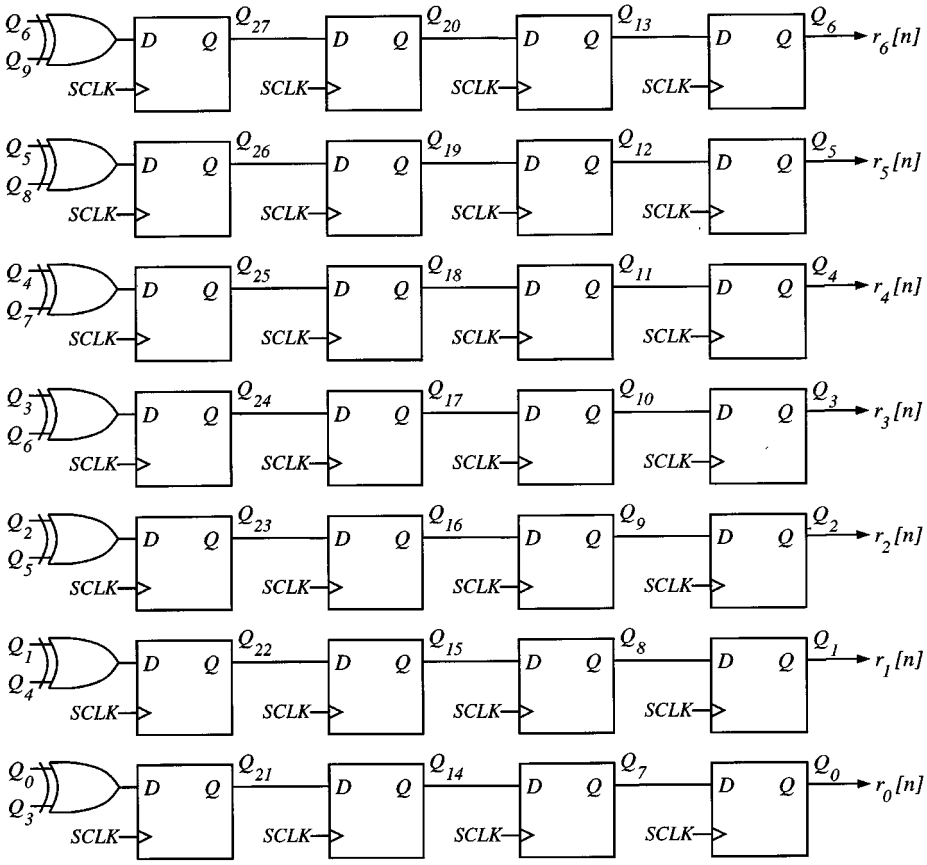


Fig. 9. The "type-I" LFSR of Fig. 8 modified to advance from state n to state $n+7$ on each clock cycle.

in the flash ADC are swapped according to a single-bit random sequence. The swapping is performed by transmission gates arranged such that the sign of each comparator offset is modulated by the random sequence but the polarity of the signal is unaffected. Only one threshold is active in the ADC per sample, so the random sequence only affects one comparator in the ADC per sample. Thus, a single random sequence is sufficient for the entire comparator bank.

It can be shown that comparator offset DEM causes the offset errors to appear as white noise and attenuated spurious components [22]. Though it does not completely whiten spurious tones caused by offset errors, it was verified through simulations that comparator offset DEM along with the attenuation of the noise transfer function was sufficient to achieve better than 105-dB SFDR.

E. Pseudorandom Sequence Generator

The mismatch-shaping DAC digital encoder and flash ADC require a total of seven single-bit pseudorandom sequences. To avoid introducing periodic artifacts in the 10 Hz–24 kHz audio band, the sequences must have a repeat rate well below 10 Hz and must be mutually uncorrelated for time shifts up to 100 ms. Though a linear feedback shift register using 19 D-flip-flops can generate a single pseudorandom sequence with a period of 170 ms, taking seven adjacent bits from an LFSR will result in signals that are merely delayed versions of each other. Though the correlation can be reduced by using a so-called "type-II" LFSR, this implementation does not provide sufficiently low correlation between the pseudorandom sequences for this application.

Seven separate LFSR's with differing lengths or with carefully chosen initial conditions could be used to provide uncorrelated sequences, but this approach would require on the order of 140 D-flip-flops.

Alternatively, the seven uncorrelated sequences could be obtained from a single LFSR clocked seven times per sample period because a single-bit sequence taken from an LFSR approximates a white random sequence. Fig. 8 shows an example of such a circuit [23]. The increased clock rate implies that the period of each sequence is reduced by a factor of seven. Thus, a minimum of 22 D-flip-flops are necessary to keep the period of

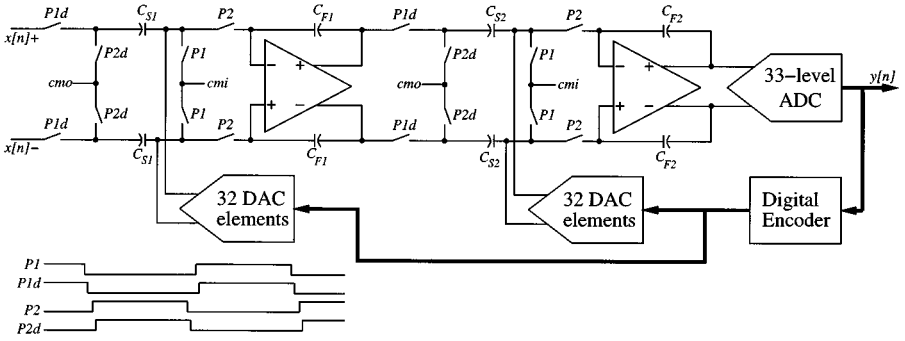


Fig. 10. The circuit-level $\Delta\Sigma$ modulator topology. $C_{S1} = 4.35$ pF, $C_{F1} = 25.28$ pF, $C_{S2} = 12.64$ pF, and $C_{F2} = 6.53$ pF.

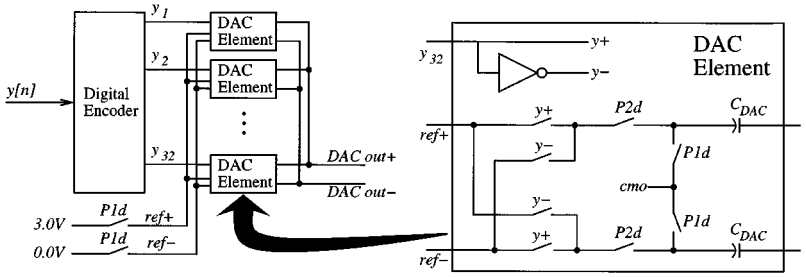


Fig. 11. The DAC bank circuit topology. $C_{\rm DAC} = 136$ fF.

each sequence above 100 ms. The drawback to this approach is the requirement for a clock signal at seven times the sample clock.

To circumvent this problem, the state update logic of the circuit in Fig. 8 can be modified to cause the LFSR to jump from state n to state $n+7$ on each clock cycle. It follows from Fig. 8 that $Q_{27}[n+1] = Q_0[n] \oplus Q_3[n]$. Noting that the shift register connection of the D-flip-flops in Fig. 8 implies $Q_k[n+m] = Q_{k+m}[n]$, for $0 \le k \le 27$ and $-k \le m \le 27-k$, the state at time $n+7$ can be written in terms of the state at time n as follows:

$$Q_k[n+7] = \begin{cases} Q_{k+7}[n], & 0 \le k < 21 \\ Q_{k-21}[n] \oplus Q_{k-18}[n], & 21 \le k \le 27. \end{cases}$$

The modified circuit, shown in Fig. 9, implements the state update logic above. Thus, it is logically equivalent to the circuit in Fig. 8 clocked at seven times the sample rate but avoids the need for a high-rate clock. It generates seven sequences that are uncorrelated for time shifts up to 12.46 s using 28 D-flip-flops and seven exclusive-OR gates. Though the LFSR was implemented off-chip to facilitate experimentation, it requires little hardware and could easily be integrated on-chip.

III. Circuit Implementation Details

A. Switched-Capacitor Circuits

The $\Delta\Sigma$ modulator was implemented using two delaying, fully differential, switched-capacitor integrators as shown in Fig. 10. The use of two delaying integrators decouples their settling behavior and simplifies their design. The 2.8-V peak differential input voltage was chosen to accommodate typical line-level audio signals. The DAC operates with 3.0- and 0-V references, and the flash ADC uses 2.0- and 1.0-V references; this choice of reference levels provides an implicit gain of three from the flash ADC input to the DAC output in Fig. 10.

The output of the mismatch-shaping DAC digital encoder controls both of the 32-element DAC arrays, and each DAC element is implemented as a differential switched-capacitor pair, as shown in Fig. 11. The DAC capacitors are sized such that $32C_{\rm DAC} = C_{S1}$. By discharging the entire array on phase 1 (*P1*) and connecting each DAC element to the references in a normal or an inverted sense on phase 2 (*P2*), the DAC provides 33-level feedback to each integrator. This implementation avoids signal-dependent reference loading that can generate second harmonic distortion. Four transmission gates are required per DAC element, and they are placed on the bottom-plate side to keep the summing nodes of the integrator as small and well shielded as possible.

It can be shown that the input-referred thermal noise contribution of the first-stage DAC and sampling capacitors is

$$\bar{V}_{\rm th} = \sqrt{\frac{8kT}{C_{S1}M}}$$

where k is Boltzmann's constant, T is the temperature in Kelvin, C_{S1} is the sampling capacitance, and M is the oversampling ratio. Thus, for a 2.8-V peak, differential input and $M = 64, C_s = 4.35$ pF is sufficient to achieve a 105-dB signal-to-thermal-noise ratio at 27 C. This implies $C_{\rm DAC} = 136$ fF.

Metal–metal capacitors were chosen over MOSCAP's, since the best SINAD performance reported for MOSCAP-based switched-capacitor circuits to date is below 90 dB [24], [25]. The metal–metal capacitors use a three-layer parallel-plate structure, with metal 3 and metal 1 forming the parasitic "bottom plate" and metal 2 forming the nonparasitic "top plate." The first-stage feedback capacitors and second-stage

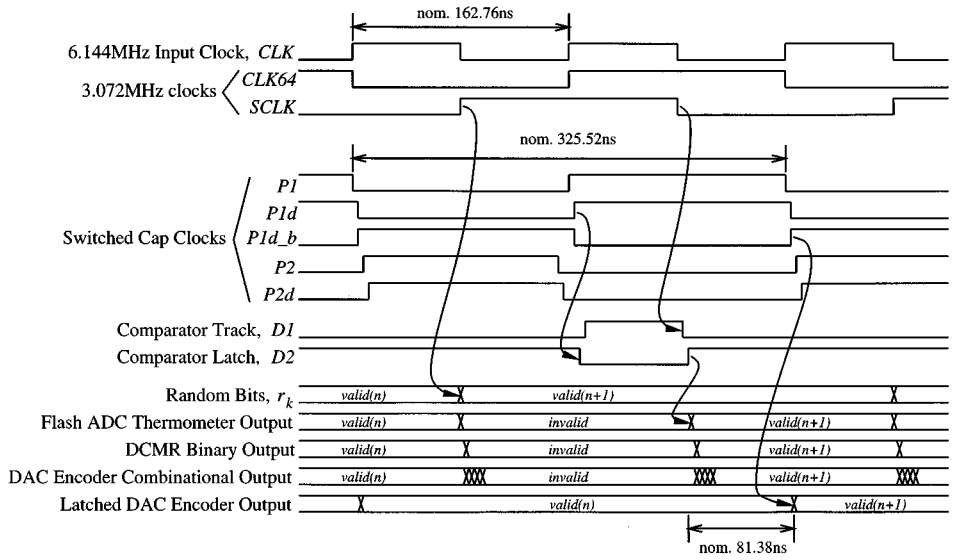
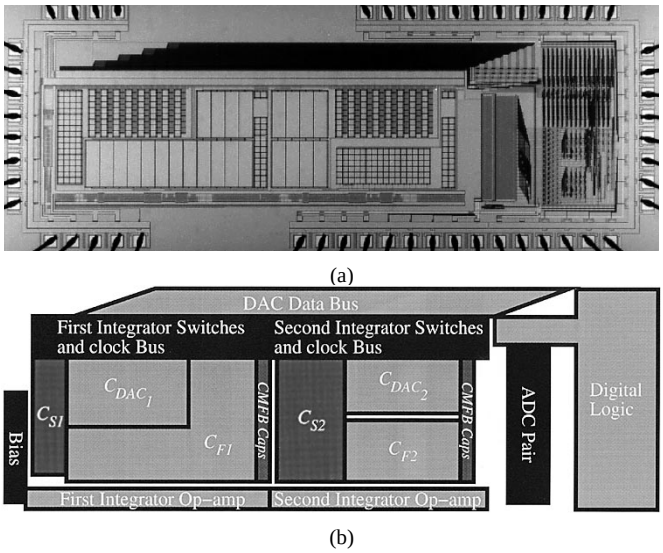


Fig. 12. Timing diagram for $\Delta\Sigma$ modulator prototype's switched-capacitor circuits and digital logic.



(a)

(b)

Fig. 13. Die photograph and layout floorplan.

TABLE I
PERFORMANCE AND SPECIFICATION SUMMARY

Sample Rate	3.072MHz
Oversampling Ratio	64
Full-scale input range	±3.0V peak differential
Peak SINAD	98.1dB at 2.8V, 10Hz–24kHz
SFDR	105dB, 10Hz–24kHz
DR	99.4dB, 10Hz–24kHz
Power dissipation	66mW analog, 2.6mW digital
Technology	3.3V, 0.5μm CMOS (1 poly, 3 metal)
Chip size	5mm × 1.9mm
Package	65 pin PGA

sampling capacitors use 3.16-pF unit capacitors measuring 112 by 369 μm^2 with a bottom-plate parasitic capacitance of 1.62 pF. All other capacitors use a 136-fF unit capacitor measuring 46 by 46 μm^2 with a bottom-plate parasitic capacitance of 126 fF. The 136-fF unit capacitors use a poly layer tied to a quiet 0-V potential as a bottom-plate shield, while the 3.16-pF capacitors use an N-well shield. The poly shield was used under the smaller unit capacitors to provide better shielding of the most sensitive nodes at the expense of higher parasitic capacitance, while the N-well shield was used under the feedback and second-stage sampling capacitors to reduce their parasitic capacitance.

The integrators use single-stage folded-cascode operational transconductance amplifiers with differential gain enhancement [26]. The amplifiers are designed for exponential settling without slew-rate limiting, and the output swing is modest to keep the dc gain relatively constant over the entire output range. Over temperature, supply, loading, process corners, and the 1-V peak differential output range, simulations show that during *P1* the first integrator has >118-dB dc gain, >40.5-MHz unity-gain bandwidth, and >57° phase margin. During *P2*, it has >106-dB dc gain, >13.9-MHz unity-gain bandwidth, and >112° phase margin.

The switch sizes were chosen to allow adequate settling while minimizing distortion and susceptibility to coupled noise. As a result, the on-resistance of the switches limits the settling behavior. The summing node switches were sized small to limit the bandwidth of the sampling networks and to minimize their charge injection. The input transmission gates were sized to provide sufficiently low on-resistance over the entire input signal range.

SPICE transient simulations were used to verify the integrators' settling behavior on *P1* and *P2*. To verify that incomplete settling did not lead to appreciable distortion, eight SPICE transient simulations of the full $\Delta\Sigma$ modulator were run in parallel for 8192 clock cycles with different initial conditions. These simulations used a combination of transistor-level simulation of the critical switched-capacitor circuits and behavioral modeling of the remaining circuits to reduce simulation time. The 8192-point power spectral density estimate obtained by averaging the periodograms taken from each of these runs verified that the harmonic distortion was better than 100 dB below the 10-kHz full-scale input signal.

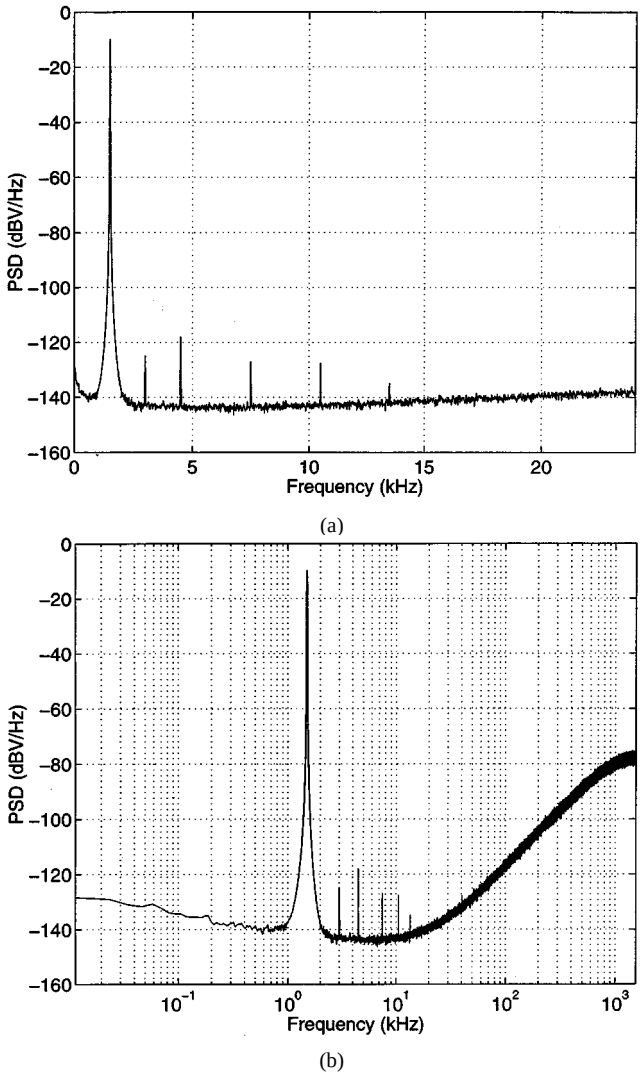


Fig. 14. Power spectral density; 1.5-kHz, 2.8-V peak differential input. (a) 0 Hz–24 kHz and (b) 0 Hz–1.536 MHz.

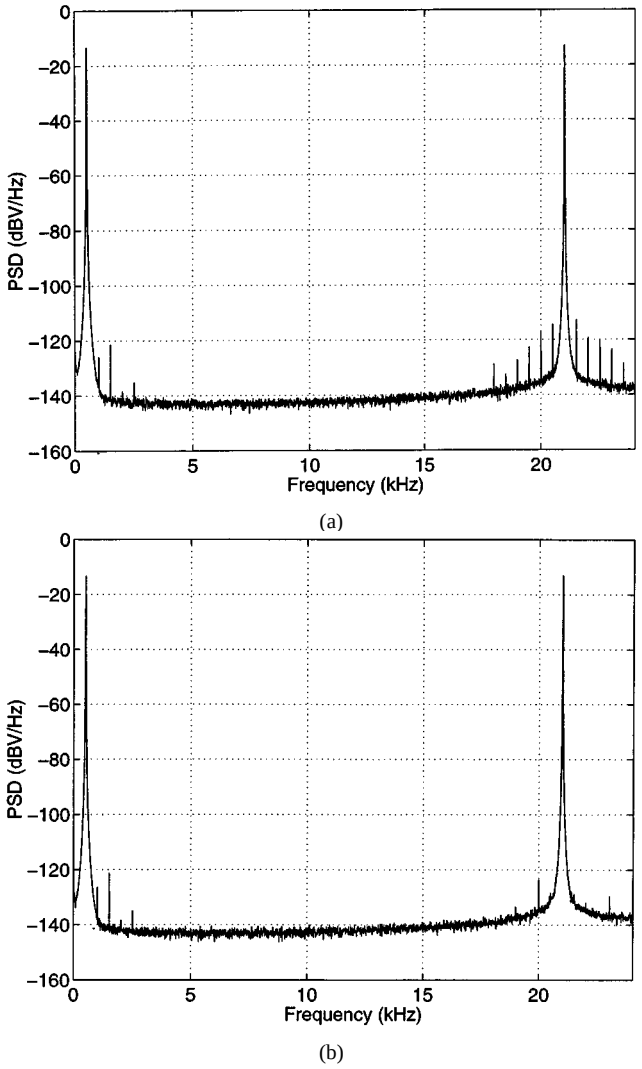


Fig. 15. Power spectral density; 500-Hz, 21-kHz two-tone, 2.8-V peak differential input. (a) Comparator offset DEM disabled and (b) comparator offset DEM enabled.

Established high-performance switched-capacitor techniques such as delayed bottom plate switching [27] and isolation of analog and digital switching events were used. The digital cells and output pads were designed for modest switching speed to minimize noise generation. The substrate ties for all digital circuits and output drivers were kept separate from the current-bearing V_{ss} lines to reduce noise coupling into the substrate. Four on-chip supply domains were used to isolate the switched-capacitor amplifiers and switches from the switched-capacitor clock generation and switch driver circuits, the flash ADCs, and the digital logic. This conservative approach was used because even synchronous, signal-independent switching noise from "clean" circuits such as the nonoverlapping clock generator can create distortion when coupled into the input through the signal-dependent on-resistance of the sampling network.

B. Digital Logic Circuits

The $\Delta\Sigma$ modulator's 6.144-MHz input clock is divided on-chip to produce a pair of 3.072-MHz clock signals. One clock drives the switched-capacitor nonoverlapping clock generator to produce *P1*, *P1d*, *P1_b*, *P2*, and *P2d* shown in Fig. 12. The other clock signal *SCLK* updates the state of the pseudorandom sequence generator, the requantizer state machine, and the switching blocks.

The switched-capacitor topology in Figs. 10 and 11 implies that the flash ADC pair must sample the second integrator's output at the end of *P1* and that the switched-capacitor DAC element select lines must be stable by the beginning of the following *P2* cycle. This was accomplished by sampling the second integrator's output halfway through the *P1* clock phase as shown in Fig. 12 to allow the remainder of the *P1* cycle for digital processing. Because the second integrator is simply holding its output during *P1*, no additional settling error is incurred by sampling at the midpoint rather than at the end of *P1*. The nonoverlapping clock generator for the comparators is driven by $P1d \cdot SCLK$, where "$\cdot$" denotes the logical AND operation. Thus, the flash ADCs track during the first half of *P1* and are latched for the remainder of *P1* and *P2*.

Once the flash ADC's comparator outputs are latched, the data path through the thermometer-to-binary decoder, digital

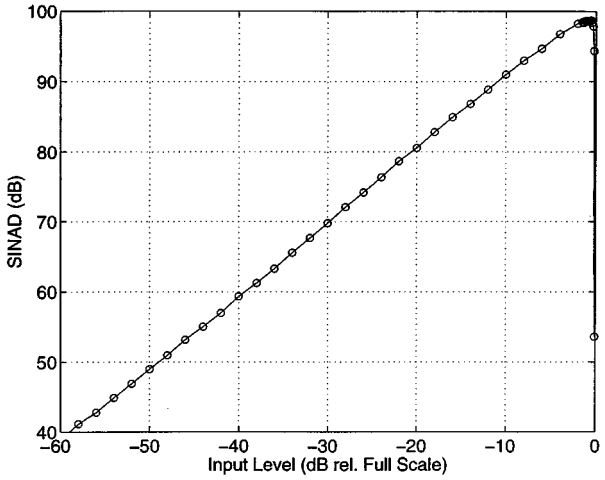


Fig. 16. 1.5-kHz SINAD versus input level.

common-mode rejection, and switching blocks consists only of combinational logic. The combinational output of the mismatch-shaping DAC encoder is clocked into a register bank on the rising edge of *P1d_b*, as shown in Fig. 12, to provide stable select signals for the switched-capacitor DAC elements. The longest propagation delay observed through the combinational path in simulation under worst case process, temperature, and loading conditions was under 50 ns. Thus, the digital processing is completed well within the 81-ns time window from the time when valid flash ADC data is available to the time of the rising edge of *P1d_b*.

IV. Prototype Results

Reducing analog complexity and capacitor area at the cost of increasing the digital complexity resulted in net area savings. From the floorplan and die photograph shown in Fig. 13 and the performance summary in Table I, it can be seen that the area and power are dominated by the switched-capacitor circuits. The capacitor area that would be required to implement a switched-capacitor differential input flash ADC is roughly equal to the DAC array. It can be seen from Fig. 13 that this capacitor array would have been double the size of the single-ended flash ADC used in this design. The additional digital logic to implement the mismatch-shaping DAC, digital common-mode rejection, and comparator DEM occupy only 14% of the total chip area and consume 4% of the total power.

As implemented in the prototype, the digital common-mode rejection flash ADC was approximately 13% smaller than the switched-capacitor differential flash ADC described in Section III. Because the area required for digital common-mode rejection is dominated by digital logic, improvements in digital layout and reduced device geometries will result in further area savings over the switched-capacitor approach. For example, it is estimated that the area of the DCMR flash ADC can be reduced by logic minimization and improved digital layout to make it 40% smaller than the switched-capacitor flash ADC.

The prototype achieves 98-dB peak SINAD for single-tone audio-band inputs and 105-dB SFDR for single- and two-tone inputs. These results represent the worst case measured performance for a wide range of single- and two-tone audio-band inputs. Fig. 14 shows the power spectral density for a 2.8-V peak, differential input signal at 1.5 kHz. The third harmonic is 105 dB below the fundamental and limits the $\Delta\Sigma$ modulator's SFDR. The $\Delta\Sigma$ modulator also has excellent small-signal performance with a measured dynamic range (DR) of 99.4 dB.

To demonstrate the reduction of spurious tones provided by comparator offset DEM, Fig. 15 shows the power spectral density with and without DEM for a full-scale, two-tone, 500-Hz, 21-kHz input. This two-tone input was chosen because the intermodulation products near the 24-kHz passband edge receive the least attenuation from the noise transfer function. Therefore, this particular input signal gives a clearer indication of the flash ADC's distortion than a low-frequency single-tone test. Fig. 15(a) shows the $\Delta\Sigma$ modulator's measured power spectral density with comparator offset DEM disabled. For this input, the in-band SFDR is limited to 99 dB by the second-order intermodulation product at 21.5 kHz. When comparator offset DEM is enabled, as shown in Fig. 15(b), the SFDR is improved to 108 dB.

Fig. 16 shows the $\Delta\Sigma$ modulator's SINAD versus input level and demonstrates the large no-overload range of the $\Delta\Sigma$ modulator. The peak SINAD occurs at −0.5 dB relative to the full-scale digital output. Thus, the $\Delta\Sigma$ modulator has an extremely wide usable input range, and no gain scaling in the decimation filter is required.

V. Conclusion

The $\Delta\Sigma$ modulator's performance demonstrates that the signal-processing innovations used in the design—mismatch-shaping multibit feedback DAC's, digital rejection of common-mode noise in the flash ADC, and DEM of comparator offsets—enable the design of high-performance ADCs in a single-poly 3.3-V CMOS process. The design approach used here shifted the design burden away from the switched-capacitor circuits at the expense of increased digital logic complexity and proved to be a successful tradeoff in a fabrication process optimized for digital logic.

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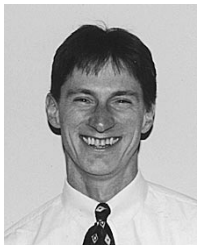

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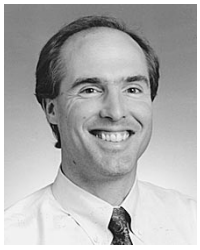

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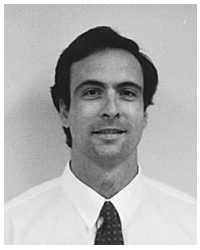

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