3 MUSOLL, E., LANG, T., and CORTADELLA, J.: 'Exploiting the locality of memory references to reduce the address bus energy'. Proc. Int. Symp. Low Power Electronics and Design, 1997, pp. 202–207
4 SHEN, A., GHOSH, A., DEVADAS, S., and KEUTZER, K.: 'On average power dissipation and random pattern testability of CMOS combinational logic networks'. Proc. IEEE/ACM Int. Conf. Computer Aided Design, 1992, pp. 402–407

Gain error correction technique for pipelined analogue-to-digital converters

E.J. Siragusa and I. Galton

A gain error correction (GEC) technique is presented that continuously measures and digitally compensates for analogue gain errors present in each stage of a pipelined analogue-to-digital-converter (ADC). Simulations with and without the GEC technique indicate that the technique results in a large improvement in the signal-to-noise-and-distortion (SINAD) and spurious-free-dynamic-range (SFDR) of the converter.

Introduction: A gain error correction (GEC) technique is presented that continuously measures and digitally compensates for analogue gain errors present in each stage of a pipelined analogue-to-digital-converter (ADC). In this Letter, the four-stage pipelined ADC in Fig. 1 is used to demonstrate the GEC technique. Except for the last stage which contains only a 33 level flash ADC, each stage of the pipeline contains a 17 level flash ADC, a 17 level switched-capacitor (SC) digital-to-analogue-converter (DAC), a summing node, and an interstage gain block. The gains A_i, $i = 1$, 2, 3, represent the digital scaling necessary to correctly align the digital outputs from each stage. The analogue output of a stage, referred to as the residue, is a sign-inverted and amplified version of the stage's ADC quantisation noise. Subsequent stages of the pipeline digitise the residue, and the digital outputs of all the stages are combined. Ideally this generates a high precision digital representation of the input signal.

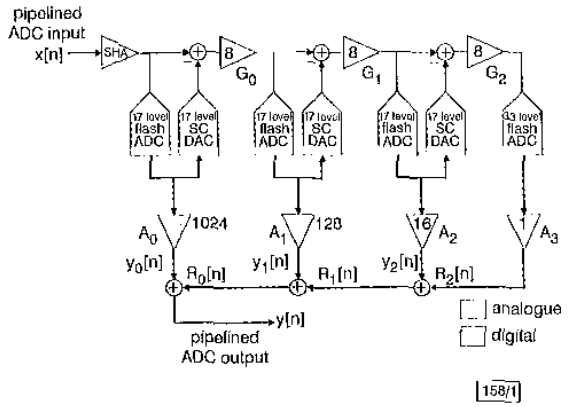

Fig. 1 *Example four-stage pipelined ADC*
Delays not shown

For the purpose of demonstrating the GEC technique it is assumed throughout this Letter that gain errors are the dominant contributors to the overall pipelined ADC error. In particular, it is assumed that the sample-and-hold-amplifier (SHA) at the converter input and the op-amps in the switched-capacitor circuits do not limit the overall performance. It is also assumed that the DAC signal-dependent errors (which are usually the dominant source of error [1]) have been corrected for by another technique such as that presented in [2]. It can be shown that each stage's ADC errors have virtually no effect on the overall pipelined ADC performance provided they do not cause the input range of the following stage to be exceeded [1]. To leave a margin for the flash ADC errors, the interstage gains are chosen such that the maximum swing of the residue, in the absence of flash ADC errors, is half the allowable input range of the next stage.

GEC technique: As shown below, gain errors cause incomplete cancellation of the quantisation noise from each stage's coarse ADC, which leads to a reduction in the overall converter's signal-to-noise-and-distortion (SINAD) and spurious-free-dynamic range (SFDR). For example, errors in the DAC gain and interstage gain in the first stage, and the error in the overall gain in the remaining stages cause the quantisation noise from the first stage's ADC to not be completely cancelled.

A simplified example wherein the GEC technique is applied only to the first stage is shown in Fig. 2. Stages 2–4 constitute a pipelined ADC in their own right and are modelled as a single ADC. To implement GEC a pseudorandom ±1 signal $r_0[n]$ is scaled by $\frac{1}{4}$ and added to the output of the first-stage ADC in order to travel the same paths that the first-stage quantisation noise travels. Note that the resolution of the DAC must be increased to accommodate the $\pm\frac{1}{4}$ signal, and half the extra input range of the next stage is consumed.

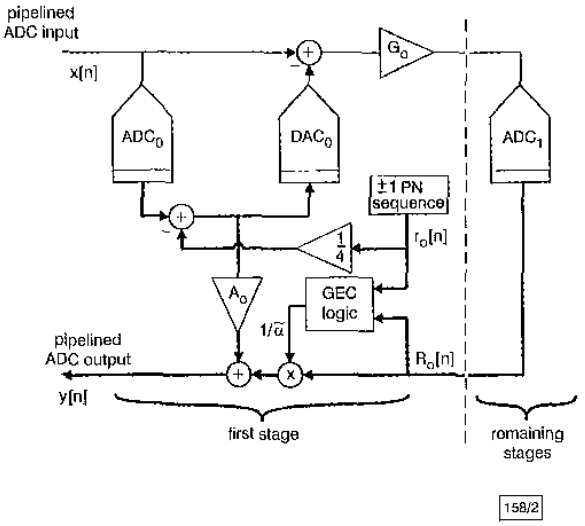

Fig. 2 *Simplified model of pipelined ADC with GEC*

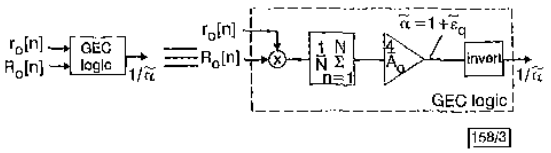

Fig. 3 *GEC logic*

The details of the block labelled GEC logic are shown in Fig. 3. The digitised residue of the first stage, $R_0[n]$, is correlated against $r_0[n]$ and scaled to obtain an estimate of the normalised gain, called $\tilde{\alpha}_q$, in the path travelled by the quantisation noise. Thus

$$\tilde{\alpha}_q = \left(\frac{1}{A_0/4}\right)\frac{1}{N}\sum_{n=1}^{N} R_0[n]r_0[n] = 1 + \tilde{\varepsilon}_q \qquad (1)$$

where N is the total number of samples in the correlation and $\tilde{\varepsilon}_q$ is the gain error estimate. The digitised residue is then divided by the gain estimate to better eliminate the first-stage quantisation noise in the final output.

Behavioural C-language simulations of the pipelined ADC were performed using realistic values for non-ideal circuit behaviour. The reference voltages for each flash ADC were generated by a simulated resistor ladder wherein each resistor was chosen with a random error of 0.3% standard deviation, and the offset voltage of each comparator in the ADC was chosen randomly with a standard deviation of 10 mV. For the first stage DAC and first-stage interstage gain, fixed errors of +0.5% were chosen to give a worst case condition where the gain errors have the same polarity. The interstage gains for the second and third stages were chosen with a random error of 0.3% standard deviation. Except for the first-stage DAC gain error, the first and second stage DACs were ideal, as it was assumed that another technique was used to correct them

if necessary. Mismatches in the third stage 17 level DAC were modelled by selecting the two output voltages corresponding to each 1 bit DAC with random errors of 0.3% standard deviation.

Fig. 4 shows the power spectral density (PSD) of the converter output before and after application of the GEC technique. Use of the GEC technique resulted in a 17dB improvement in SINAD and a 28dB imprdvement in SFDR. The number of samples used in the correlation to produce the gain estimate was 2^{25}. For a 10MHz sample rate converter, this corresponds to a 3.2 second warm-up period, during which the converter can still be operated normally. The PSDs were performed on the converter output data after completion of the warm-up period.

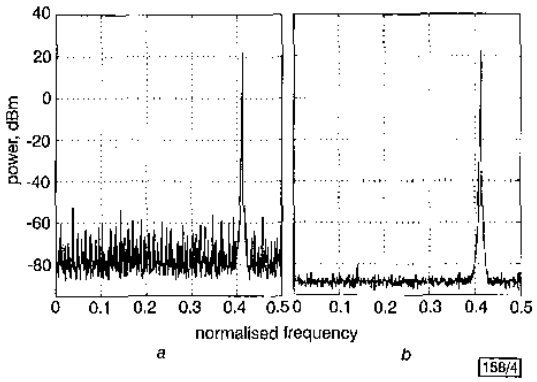

Fig. 4 *Power spectral density of output of pipelined ADC*
a Without GEC
b With GEC

Theory: In the absence of GEC, it can be shown using Fig. 2 that the overall pipelined ADC output is

$$y[n] = \alpha_x x[n] + A_0[1 - \alpha_q]e_{q0}[n] + \alpha_d e_{d0}[n] + e_{q1}[n] \quad (2)$$

where $x[n]$ is the input to the converter, $e_{q0}[n]$ is the first-stage quantisation noise, $e_{d0}[n]$ is the first-stage DAC noise error, $e_{q1}[n]$ is the quantisation noise from the remaining stages, α_x is the overall pipelined ADC converter gain, α_d is the gain from the DAC output to the overall pipelined ADC converter output, and α_q is the gain from the ADC output to the digitised residue. With GEC, it can be shown that the corrected output is

$$y[n] = \alpha_{x'} x[n] + A_0\left[1 - \frac{\alpha_q}{\tilde{\alpha}_q}\right]\left(e_{q0}[n] + \frac{r_0[n]}{4}\right) + \frac{\alpha_d}{\tilde{\alpha}_q}e_{d0}[n] + \frac{e_{q1}[n]}{\tilde{\alpha}_q} \quad (3)$$

where $\alpha_{x'}$ is the new converter gain, which is approximately equal to α_x. Thus for perfect gain estimation, $e_{q0}[n]$ is completely cancelled. The GEC also causes slight changes to the coefficients of the other signals, which is usually acceptable as it does not significantly degrade the SINAD or SFDR.

Provided that $r_0[n]$ is uncorrelated with the other signals present in $R_0[n]$, it can be shown that $\tilde{\alpha}_q$ is an unbiased estimator for α_q and that the law of large numbers guarantees its convergence with probability 1 as the number of samples taken in the correlation approaches infinity. Therefore, in the limit as $N \to \infty$, $e_{q0}[n]$ is completely cancelled. In practice the number of samples chosen for the length of the correlation depends on the magnitude of $r_0[n]$ relative to the magnitudes of the other signals in $R_0[n]$, and how close $\tilde{\alpha}_q$ is required to be to α_q.

Implementation issues: Although a specific simplified example has been shown, the GEC technique can be applied to other pipelined ADC architectures, and it can be applied to more than one stage. Other magnitudes of the random signal may also be used, as long as the input range of the next stage is not exceeded. To avoid increasing the resolution of the DAC, the random signal can be added to the input of a stage's ADC instead of at its output. However, since the gain of the ADC would be in the path of the random signal, an additional correlation would be needed at the stage's digital output in order to determine this gain. This random signal can be created by adding an offset to the ADC that can be toggled. For example, the number of resistors in the reference ladder for the flash ADC can be increased (without changing the total resistance) and the reference inputs of the comparators can be randomly switched up or down the ladder to produce the offset.

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References

1 LEWIS, S.H., and GRAY, P.R.: 'A pipelined 5-Msample/s 9-bit analog-to-digital converter', *IEEE J. Solid State Circuits*, 1987, **SSC-22**, (6), pp. 954–961
2 GALTON, I.: 'Dynamic noise cancellation in pipelined analog-to-digital converters', *to be published in IEEE Trans. Circuits Syst. II*,

Accurate modelling of planar microwave circuit using conformal FDTD algorithm

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A conformal finite difference time domain (CFDTD) algorithm is presented for accurately modelling perfectly conducting curved objects and illustrated by applying it to a circularly shaped radial stub.

Introduction: While the finite difference time domain method (FDTD) has been very successfully used to model various electromagnetic phenomena [1], its application to complex, non-Cartesian geometries has been rather limited owing to the errors caused by staircasing of the geometry. Although a number of attempts have been made to alleviate the staircasing problem [2, 3] by using a conformal FDTD scheme, the difficulties of complex mesh generation and the problem caused by the instability of the algorithm persist, because of the use of distorted cell areas in the update algorithm. In contrast, the conformal technique proposed in this Letter neither requires any modifications of Yee's FDTD difference equations, nor does it employ distorted cell areas, but instead uses the length of the distorted cell side in the update equations for the magnetic fields. The conformal algorithm presented in this work can be used to accurately model perfect electric conductor (PEC) objects with curved surfaces and edges, is computationally efficient and numerically stable.

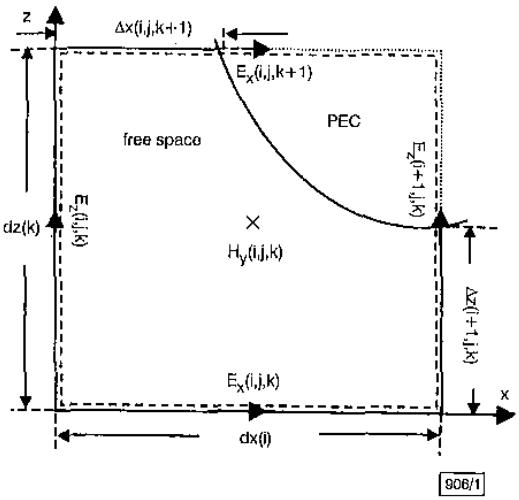

Fig. 1 *Intersection between FDTD mesh and PEC in x-z plane*