An Audio ADC Delta-Sigma Modulator with 100dB SINAD and 102dB DR Using a Second-Order Mismatch-Shaping DAC

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Abstract

A second-order audio ADC $\Delta\Sigma$ modulator using a low-complexity 33-level second-order mismatch-shaping DAC is presented. The DAC encoder is designed to reduce signal-dependent DAC noise modulation. The prototype was implemented in a 3.3V 0.5μm single-poly CMOS process, and it achieves 100dB SINAD and 102dB DR.

Introduction

Multibit $\Delta\Sigma$ modulation has recently been applied to implement high-performance $\Delta\Sigma$ADCs [1]–[3]. A multibit $\Delta\Sigma$ modulator can achieve the same signal to quantization noise ratio as a 1-bit $\Delta\Sigma$ modulator with a lower modulator order and a reduced oversampling ratio. These benefits can be used to relax the performance requirements on the analog switched-capacitor circuitry and enable the implementation of high-performance $\Delta\Sigma$ADCs in digital-optimized CMOS fabrication processes [3]. However, realizing these benefits requires an internal DAC with the same inband precision as the $\Delta\Sigma$ADC.

The development of mismatch-shaping DACs has helped make the implementation of multibit $\Delta\Sigma$ADCs practical. While several mismatch-shaping algorithms have been reported that provide first-order spectral shaping of static DAC mismatch errors [4]–[10], only a few provide second-order mismatch shaping [8]–[11]. Though [8] and [9] show simulated second-order mismatch shaping, detailed hardware-level implementations are not presented.

While second-order mismatch shaping algorithms theoretically offer increased inband precision over first-order algorithms, they present several challenges. The encoder's increased complexity must not outweigh its performance gains. The switching or selection logic, which is based on $\Delta\Sigma$ modulation in [8]–[11], must be stable for real-world input signals. The encoder should minimize spurious tones in the DAC noise and signal-dependent DAC noise modulation because these effects can limit the dynamic range of high-resolution $\Delta\Sigma$ADCs.

This paper presents a second-order audio ADC $\Delta\Sigma$ modulator using a second-order mismatch-shaping DAC encoder based on the tree structure in [10] that addresses these challenges. The prototype $\Delta\Sigma$ modulator uses the analog front end circuitry presented by the authors in [3] with a redesigned mismatch-shaping DAC encoder. The DAC encoder uses an improved version of the second-order sequencing logic simulated in [9]. The modifications presented here reduce its hardware complexity and provide graceful degradation to first-order shaping under overload conditions. The tree-structured encoder employs a modified input layer block to reduce signal-dependent DAC noise modulation and improve SNR for low-level input signals. The prototype $\Delta\Sigma$ modulator is implemented in a standard 0.5μm, 3.3V single-poly CMOS fabrication process. All twelve of the fabricated prototypes achieve 100dB peak SINAD and 102dB dynamic range over the 10Hz-20kHz audio band.

Mismatch-Shaping DAC Signal Processing

The prototype uses the second-order $\Delta\Sigma$ modulator architecture shown in Fig. 1 with 33-level quantization and feedback. The 33-level mismatch-shaping DAC encoder is based on the tree structure presented in [10]. The five layer binary input tree structure shown in Fig. 2 drives the 33-level unit element DAC array. The layers of the DAC encoder are labelled 5 through 1; *layer 5* denotes the input layer and *layer 1* denotes the output layer. As shown in Fig. 2, each layer, k, of the encoder has 2^{5-k} elements. The nodes in the encoder are referred to as *switching blocks* and are denoted $S_{k,r}$, where k denotes the encoder layer and r denotes the position within the layer. Each switching block has one input, $x_{k,r}[n]$, and two outputs, $x_{k-1,2r}[n]$ and $x_{k-1,2r-1}[n]$.

The *switching sequences*, $s_{k,r}[n]$, are generated within the switching blocks as shown in Fig. 3 and determine the spectral shaping of the DAC noise. The sequence $d_k[n]$ is an i.i.d. sequence of uniform random variables on $(-1,1)$. The switching sequences are constrained by the requirements that the encoder's 1-bit outputs must sum to the encoder's input and that $0 \le x_{k,r}[n] \le 2^k$. Restricting $s_{k,r}[n] = 0$ for $x_{k,r}[n]$ even and $s_{k,r}[n] = \pm 1$ for $x_{k,r}[n]$ odd is sufficient to meet these requirements. For the tree-structured mismatch-shaping DAC with input $x[n]$ and output $y[n]$, it is shown in [10] that $y[n] = \gamma x[n] + \beta + e[n]$, where

$$e[n] = \sum_{k=1}^{5} \sum_{r=1}^{2^{5-k}} \Delta_{k,r} s_{k,r}[n],$$

and γ, β, and $\Delta_{k,r}$ are constants which depend only on the static DAC mismatches. If the switching sequences are all uncorrelated and have the same spectral characteristics (e.g. second-order spectral shaping), then $e[n]$, referred to as *DAC noise*, will also possess this spectral shaping.

Second-Order Switching Block

The signal processing of the second-order switching block is shown in Fig. 3. This switching sequence generator with feedforward gain $\alpha = 8$ and $d_k[n] = 0$ was used to generate the simulation results shown in [9] though the circuit itself was not published. The switching sequence generator is analogous to a digital $\Delta\Sigma$ modulator with a zero input. The multiplier following the comparator in Fig. 3 uses $x_{k,r}^{(0)}[n]$, the LSB of $x_{k,r}[n]$, to force $s_{k,r}[n] = 0$ for even $x_{k,r}[n]$.

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Unlike the first-order switching blocks in [3] and [10], the second-order switching sequence generator in Fig. 3 can exhibit instability. For example, if the first integrator's output, $I_1[n]$, is nonzero and a sequence of even inputs occurs, the second integrator's output, $I_2[n]$, will continue to grow in magnitude until an odd input occurs. Unless restrictions are placed on the occurances of even values of $x_{k,r}[n]$, no bound can be placed on $|I_2[n]|$. Therefore, the number of bits required to represent $I_1[n]$ and $I_2[n]$ depends on the choice of α and the statistics of $x_{k,r}[n]$.

A simplified implementation of the switching sequence generator shown in Fig. 3 can be obtained by observing that in simulations $s_{k,r}[n]$ retains second-order spectral shaping for values of $\alpha > 8$. Thus, if $|I_1[n]| \leq M$ and $|I_2[n]| \leq M$, a gain of $\alpha > M$ can be implemented by allowing $I_1[n]$ to override $I_2[n]$ whenever $I_1[n]$ is nonzero. The gain element, adders, and comparator in Fig. 3 can then be replaced by the following decision logic:

$$Q[n] = \begin{cases} +1 & I_1[n] > 0 \text{ or} \\ & I_1[n] = 0 \ \& \ I_2[n] > 0 \text{ or} \\ & I_1[n] = I_2[n] = 0 \ \& \ r_k[n] = 1; \\ -1 & I_1[n] < 0 \text{ or} \\ & I_1[n] = 0 \ \& \ I_2[n] < 0 \text{ or} \\ & I_1[n] = I_2[n] = 0 \ \& \ r_k[n] = 0, \end{cases} \quad (1)$$

where $r_k[n]$ is an i.i.d. dither sequence with $P(r_k[n] = 1) = P(r_k[n] = 0) = 1/2$. For this choice of decision logic, $I_1[n]$ only takes on the values in the set $\{-1, 0, 1\}$, and a two-bit accumulator is sufficient to implement I_1. Fig. 4 shows the simplified second-order switching block incorporating the decision logic in (1) as well as hardware simplifications presented in [3]. The I_1 and I_2 accumulators are designed such that they saturate at their extreme values rather than "rolling over".

The implementation in (1) ensures that I_1 continues to control $s_{k,r}[n]$ when I_2 saturates. Thus, in this overload condition, the switching sequence generator degrades to first-order spectral shaping until I_2 recovers from saturation. Because of this benign overload behavior, the bit-width of I_2 can be reduced at the expense of minor degradation of the spectral shaping near dc. Fig. 5 shows the DAC noise PSD for various I_2 bit widths. This plot shows that even though encoders with four to six bits in I_2 do not yield ideal second-order shaping, they still offer significantly better performance than the first-order switching block.

Signal-Dependent DAC Noise Modulation

As implemented in Fig. 3 and Fig. 4, $s_{k,r}[n]$ is forced to zero when $x_{k,r}[n]$ is even. As a result, long sequences of even inputs to a switching block will affect the spectral shaping of $s_{k,r}[n]$. Fig. 6 shows the PSD of a single $s_{k,r}[n]$ sequence where $x^{(0)}_{k,r}[n]$ is a single-bit i.i.d. sequence with $P(x^{(0)}_{k,r}[n] = 1) = p$ and $P(x^{(0)}_{k,r}[n] = 0) = 1 - p$. Increasing the probability of even inputs dramatically changes the inband power of the $s_{k,r}[n]$ sequence. Because the DAC noise, $e[n]$, is the weighted sum of the $s_{k,r}[n]$ sequences, this directly translates to increased inband DAC noise.

For the tree structure of Fig. 2, input values that are powers of two pose a problem because they propagate even inputs to successive layers of the tree structure. A commonly-encountered input for the 33-level DAC encoder is an input of 16, the converter's midscale value. An input of 16 is factored into successive even values until the last layer and results in 15 of the 31 $s_{k,r}[n]$ sequences having significantly increased inband power.

The solid-line plot in Fig. 7 shows simulated inband noise power versus input level for the $\Delta\Sigma$ modulator of Fig. 1 using the second-order mismatch-shaping encoder shown in Fig. 2. The encoder uses the second-order switching blocks shown in Fig. 4 with 4-bit I_2 accumulators. For this implementation, the inband noise power increases by 10dB as the input drops from full-scale to -35dB. This is a direct result of the DAC encoder receiving a high density of midscale inputs. Combined with the inband thermal noise and $1/f$ noise, this level of DAC noise modulation would have limited the $\Delta\Sigma$ modulator's dynamic range to 100dB. Thus, for small input signals, second-order mismatch shaping would yield little or no improvement in SNR over first-order mismatch shaping.

This effect can be mitigated by noting that $s_{k,r}[n] \in \{-1, 0, 1\}$ is sufficient, but not necessary, to satisfy the requirements that the encoder's output sum to its input value and that $0 \leq x_{k,r}[n] \leq 2^k$. In particular, the $S_{5,1}$ block is free to set $s_{5,1}[n] = \pm 2$ for $x_{5,1}[n] \in \{4, 6, 8, \ldots 28\}$. Thus, when $S_{5,1}$ receives a long run of input value 16, it can still produce a second-order shaped $s_{5,1}[n]$ taking on values ± 2. The $S_{5,1}$ block breaks the midscale input into output values of 7 and 9 and prevents the propagation of even values to the remainder of the tree structure. The dashed-line plot in Fig. 7 illustrates the reduction in noise modulation provided by the modified $S_{5,1}$ block. The variation in inband noise is reduced from 10dB to 5dB, and the peak inband noise is reduced by 5dB.

Fig. 8 shows the $S_{5,1}$ switching sequence generator signal processing. The switching sequence generator produces $s_{5,1}[n] = \pm 1$ for odd $x_{5,1}[n]$ and $s_{5,1}[n] = \pm 2$ for $x_{5,1}[n]$ in the set $\{4, 8, 12, \ldots 28\}$. Though this modification increases the complexity of the $S_{5,1}$ block, the remainder of the tree structure uses the simple switching blocks shown in Fig. 4. Because $s_{5,1}[n]$ is no longer a 3-level signal, explicit adders must be used to produce the outputs $x_{4,1}[n]$ and $x_{4,2}[n]$. However, simplifications similar to those applied to the switching sequence generator in Fig. 4 can be used to reduce the complexity of the state machine that produces $s_{5,1}[n]$.

Prototype Results

The prototype $\Delta\Sigma$ modulator IC shown in Fig. 9 was fabricated in a 0.5μm, 3.3V, triple-metal, single-poly CMOS process. The analog front end of the prototype — the switched-capacitor circuitry and flash ADCs with comparator offset DEM and digital common mode rejection (DCMR) — are identical to the audio ADC $\Delta\Sigma$ modulator using a first-order mismatch shaping DAC presented by the authors in [3]. Logic reduction and layout optimization were performed on the DCMR logic

to reduce its area. Though the second-order mismatch-shaping DAC encoder with the modified $S_{5,1}$ block is approximately twice the die area of the first-order encoder of [3], the area reduction of the DCMR logic permitted the second-order design to fit in same pad ring as the first-order design.

Each second-order switching block shown in Fig. 4 required 31 gates, while the modified $S_{5,1}$ block in Fig. 7 required 58 gates. Thus the entire second-order mismatch-shaping DAC encoder was implemented using 988 gates. This is a lower gate count than that reported in [11] for a 9-level second-order mismatch-shaping DAC encoder.

Table 1 summarizes the device specifications and worst-case measured performance for the twelve fabricated prototypes. The $\Delta\Sigma$ modulator presented here has 1.5dB greater peak SINAD and 2.3dB greater dynamic range (DR) than the design presented [3] with no increase in die area and only a 2.6% increase in power dissipation. Fig. 9 shows measured 1.5kHz SINAD versus input level. Fig. 10 shows the measured inband PSD for -1dB and -60dB input signals.

Acknowledgment

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TABLE 1
Performance and Specification Summary

Sample Rate	3.072MHz
Oversampling Ratio	64
Full-scale input range	±3.0V peak differential
Peak SINAD	100.3dB at 2.8V, 10Hz – 20kHz
SFDR	105.6dB, 10Hz – 20kHz
DR	102.5dB, 10Hz – 20kHz
Power dissipation	66mW analog, 4.4mW digital
Technology	3.3V, 0.5μm CMOS (1 poly, 3 metal)
Chip size	5mm × 1.9mm
Package	65 pin PGA

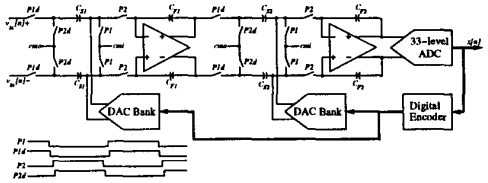

Figure 1: The switched-capacitor implementation of the second-order $\Delta\Sigma$ modulator.

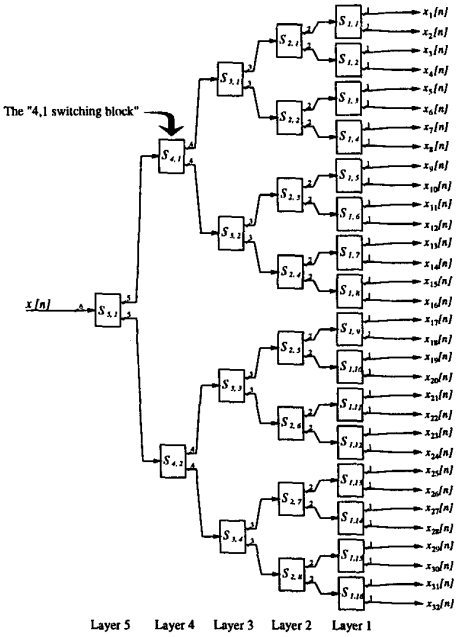

Figure 2: The 33-level tree-structured mismatch-shaping DAC encoder.

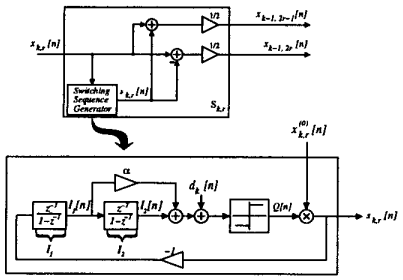

Figure 3: Second-order switching block signal processing.

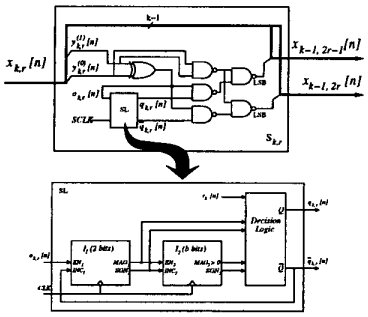

Figure 4: Second-order switching block logic-level implementation.

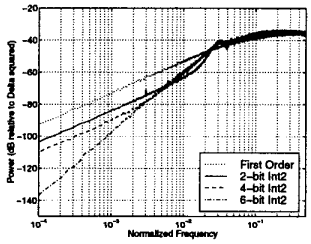

Figure 5: Simulated DAC noise PSDs for a 33-level mismatch-shaping DAC; 1st-order and 2nd-order shaping.

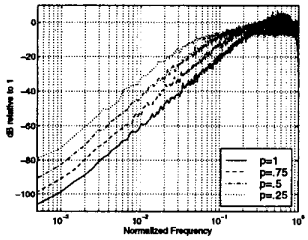

Figure 6: Simulated $s_{k,r}[n]$ sequence PSDs versus $P(x_{k,r}$ odd).

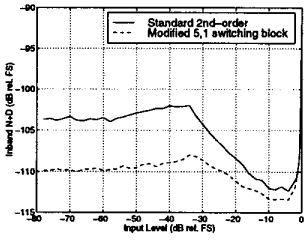

Figure 7: Simulated inband noise versus input level for the prototype $\Delta\Sigma$ modulator.

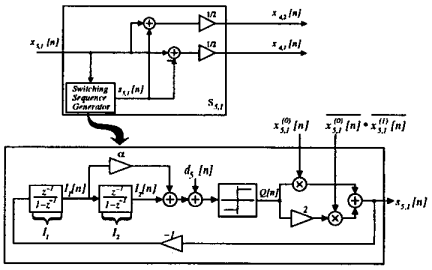

Figure 8: Modified $S_{5,1}$ switching block which allows ± 1 feedback for odd inputs and ± 2 feedback for inputs divisible by 4.

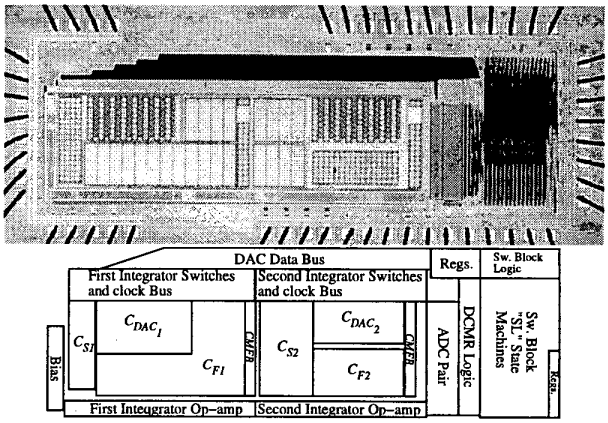

Figure 9: Prototype $\Delta\Sigma$ modulator die photograph and layout floorplan.

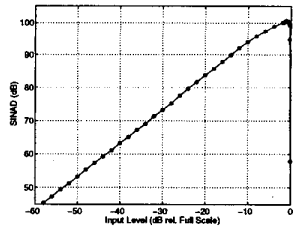

Figure 10: Measured SINAD versus input level for the prototype $\Delta\Sigma$ modulator.

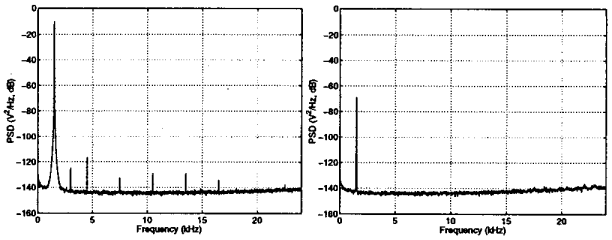

Figure 11: Measured inband PSD for -1dB and -60dB, 1.5kHz input signals.