AN AREA-EFFICIENT DIFFERENTIAL INPUT ADC WITH DIGITAL COMMON MODE REJECTION

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ABSTRACT

This paper presents a differential input flash ADC with digital common mode rejection (DCMR) and dithered, noise shaped requantization used in a high-performance, single-poly CMOS ADC $\Delta\Sigma$ modulator IC. By avoiding the use of metal-metal capacitors, the DCMR flash ADC required 14% less area than a switched-capacitor implementation and avoided circuit implementation problems. Measurements and analysis show that the DCMR flash ADC rejects common mode noise without generating spurious tones. In the absence of common mode noise, its quantization noise power is equivalent to a conventional flash ADC.

I. INTRODUCTION

The availability of mismatch-shaping multibit DACs has helped to make the implementation of high-resolution multibit $\Delta\Sigma$ADCs feasible. Compared to a single-bit design, a multibit $\Delta\Sigma$ modulator can achieve the same signal to quantization noise performance with a lower modulator order and lower oversampling ratio (OSR). The use of multibit feedback also relaxes the slew rate and settling time requirements on the analog integrators. While reducing the modulator order and OSR eases the design of the analog front end, it also reduces the noise transfer function's attenuation of noise introduced at the quantizer. Thus the performance of the internal quantizer, typically implemented as a flash ADC, can limit the $\Delta\Sigma$ modulator's performance.

High-performance ADC $\Delta\Sigma$ modulators use fully differential analog circuitry to improve the their noise immunity. To preserve the noise rejection benefits of the differential architecture, the flash ADC must quantize the loop filter's differential output and reject its common mode component. The conventional approach to differential quantization is to use a comparator bank with a pair of switched-capacitors per comparator to sample the input and reference levels on alternating clock phases [1]. However, this approach may require a prohibitively large area for a multibit $\Delta\Sigma$ modulator implemented in a CMOS process in which large area metal-metal capacitors are the only linear capacitor structures. Because the reference ladder is sampled in the switched-capacitor approach, its design is complicated by the requirement to fully charge the array of capacitors at the oversampled clock rate.

A digital common mode rejection (DCMR) flash ADC was employed in the implementation of a high-performance, single-poly CMOS $\Delta\Sigma$ modulator IC to perform differential mode quantization without the area penalty and circuit complications of the switched-capacitor approach [2]. Using a pair of single-ended, 33-level flash ADCs, the DCMR flash ADC quantizes the positive and negative portions of the loop filter's differential output. It digitally subtracts the single-ended outputs to cancel the common mode component and reduces the difference signal to 33-levels using dithered, first order shaped requantization. This technique rejects the common mode noise without generating spurious tones and provides a 33-level quantized representation of the differential signal.

II. IMPLEMENTATION IN $\Delta\Sigma$ MODULATOR

The $\Delta\Sigma$ modulator mentioned above is a second order design operating at a clock rate of 3.072MHz with an OSR of 64. Fabricated in a 3.3V, 0.5μm single-poly, triple-metal CMOS process, it achieves 98dB peak signal to noise and distortion (SINAD) and 105dB SFDR [2]. As shown in Fig. 1, it was implemented with two delaying switched-capacitor integrators, a 33-level mismatch-shaping DAC and a 33-level DCMR flash ADC. Because the noise transfer function provides only 52dB of attenuation at the 24kHz passband edge, the quantizer must provide additional common mode rejection to ensure meeting the 105dB SFDR target.

A switched-capacitor differential flash ADC of the form shown in [1] was considered for the design, but the area required and circuit challenges involved motivated the search for an alternative solution. A 33-level switched-capacitor flash ADC requires a bank of 32 comparators, an array of 64 capacitors and a 33-level thermometer-to-binary decoder. To keep the sampling capacitor large relative to the comparators' input capacitance, it must be on the order of 125fF. With the metal-metal capacitors used in the design, the sampling capacitor array is roughly three times the area of the comparator bank. Thus, the sampling capacitors dominate the flash ADC's area. Each of the 32 sampling capacitors has a bottom plate parasitic capacitance to substrate on the order of 100fF that is switched between the second integrator's output and the reference ladder on alternate clock phases. The reference ladder must be capable of fully charging these capacitances to avoid signal-dependent settling errors that give rise to distortion. The references' source resistance can be reduced by using low resistance values in the ladder, but this increases power dissipation and necessitates fast-settling, high current buffers to drive the ends of the resistor ladder. Source-followers can be used on each tap to reduce the source resistance, but the threshold voltage mismatch between devices gives rise to level-placement errors in the flash ADC that cause distortion and can limit the $\Delta\Sigma$ modulator's SINAD and SFDR.

The DCMR flash ADC shown in Fig. 2, was implemented in the $\Delta\Sigma$ modulator to avoid the area requirements and circuit difficulties described above for the

switched-capacitor approach. The DCMR flash ADC uses a pair of 33-level, single-ended flash ADCs to quantize the positive and negative portions of the second integrator's output. The outputs are converted to binary, subtracted and reduced to 33 levels by the requantization logic shown in Fig. 3. Though the DCMR flash ADC required additional circuitry — a second 33-level flash ADC, a second 33-level thermometer-to-binary encoder, an adder and requantization logic — this implementation of the DCMR flash ADC required 14% less area than the switched-capacitor approach, not including the area for reference ladder buffering. Because the DCMR flash ADC consists of comparators and digital logic implemented using minimum size devices, the DCMR flash ADC will provide further area savings over the switched-capacitor design as minimum device geometries scale downward.

Behavioral simulation results for the $\Delta\Sigma$ modulator with a full-scale sinusoidal input and a 150mV peak, 8kHz common mode signal superimposed on the second integrator's output are shown in Fig. 4. The output power spectral density (PSD) for the $\Delta\Sigma$ modulator using a single-ended flash ADC is shown in Fig. 4a to emphasize the fact that the noise transfer function alone does not provide sufficient attenuation to ensure meeting the 105dB SFDR target. Fig. 4b shows the output PSD when the DCMR flash ADC is used and the difference signal is reduced to 33 levels by truncation; though the common mode signal is attenuated, the truncation generates significant spurious tones. The configuration used in the $\Delta\Sigma$ modulator IC — the DCMR flash ADC and the dithered, first order shaped requantizer — is shown in Fig. 4c, and it can be seen that the common mode signal is rejected and that the inband SFDR is better than 110dB.

Measured common mode rejection results for the $\Delta\Sigma$ modulator IC in Fig. 5 show that the DCMR flash ADC effectively eliminates common mode noise. The output PSD for a dc input to the $\Delta\Sigma$ modulator with no common mode noise is shown in Fig. 5a, and the PSD for the same dc input with a 150mV peak, 8kHz sinusoid injected on the flash ADC's reference ladder is shown in Fig. 5b. The integrated inband noise is 100dB below the full-scale input level in both cases. No trace of the injected common mode noise can be seen in Fig. 5b, and the inband spurious components are better than 110dB below the full-scale input level.

III. SIGNAL PROCESSING DETAILS

To quantify the performance of the digital common mode rejection approach, an $(L+1)$-level DCMR flash ADC with output $y_d[n]$ followed by a $(2L+1)$-to-$(L+1)$-level requantizer is analyzed. The DCMR flash ADC is assumed to have a periodic, differential mode input with uniform dither and a common mode noise signal. To show that the common mode signal results only in modulated white noise at the output, the autocorrelation sequence, $R_{y_dy_d}[m,n] = \mathrm{E}(y_d[n]y_d[n+m])$, is calculated and is used to determine the form of the PSD, $S_{y_dy_d}(\omega)$. In the absence of common mode noise, the DCMR flash ADC is shown to have signal to quantization noise performance equivalent to a conventional $(L+1)$-level flash ADC. It is then shown that the requantization algorithm reduces $y_d[n]$ to an $(L+1)$-level signal, $y[n]$, without introducing spurious tones.

The single-ended flash ADCs within the DCMR flash ADC are of the form shown in Fig. 6. They share a resistor reference ladder driven with reference voltages $\pm\frac{V_{ref}}{2}$ and have a single-ended quantization step size, Δ, of $\frac{V_{ref}}{L}$. The single-ended ADC's quantization levels are $ref_k = k\Delta - \frac{L+1}{2}\Delta$, $k = 1, 2, \ldots L$. The $y_+[n]$ and $y_-[n]$ outputs are formed by summing the L comparator outputs and adding an offset of $-\frac{L}{2}$. Thus, each output takes on values $\{-\frac{L}{2}, -\frac{L}{2}+1, \ldots, \frac{L}{2}\}$.

By viewing each single-ended flash ADC as a gain element with gain $\alpha_q = \frac{1}{\Delta}$ followed by an additive error source, the single-ended outputs can be expressed as

$$y_+[n] = \alpha_q \frac{v'_{in,d}[n]}{2} + \alpha_q v_{cm}[n] + e_{q_+}[n],$$

and

$$y_-[n] = -\alpha_q \frac{v'_{in,d}[n]}{2} + \alpha_q v_{cm}[n] + e_{q_-}[n],$$

where $v'_{in,d}[n]$ represents the total differential mode input, $v_{cm}[n]$ represents the common mode noise and $e_{q_+}[n]$, $e_{q_-}[n]$ represent the error added by each flash ADC. The flash ADCs' output transfer functions are shown in Fig. 7a and Fig. 7b as functions of $v'_{in,d}$ for $v_{cm} = 0$, and the corresponding quantization error transfer functions are shown in dashed lines on each figure. Because the transfer functions are plotted as functions of the differential mode input, the graphs are elongated along the horizontal axis. The effect of nonzero common mode on the transfer functions is shown in Fig. 8a and Fig. 8b. Note that y_+ is shifted to the left by $2v_{cm}$ and y_- is shifted to the right by $2v_{cm}$.

The DCMR flash ADC's output, $y_d[n]$, is formed by taking the difference of the single-ended flash ADCs' outputs, giving $y_d[n] = \alpha_q v'_{in,d}[n] + e_{q,d}[n]$, where $e_{q,d}[n] = e_{q_+}[n] - e_{q_-}[n]$. The DCMR flash ADC's output and quantization error transfer functions, shown in Fig. 7c and Fig. 8c, can be computed graphically by subtracting the transfer functions for the single-ended flash ADCs. For $v_{cm} = 0$, it can be seen from Fig. 7c that the DCMR flash ADC has quantization levels $ref_k = 2k\Delta - (L+1)\Delta$, $k = 1, 2, \ldots L$ and that its output takes on $(L+1)$ output values from $\{-L, -L+2, \ldots, -2, 0, 2, \ldots, L\}$. Thus for $v_{cm} = 0$, the DCMR flash ADC behaves as an $(L+1)$-level flash ADC with quantization step size $\Delta_d = 2\Delta$ followed by a gain of two. Letting $\alpha_{q,d} = \frac{1}{\Delta_d}$, the output can be expressed for arbitrary v_{cm} as $y_d[n] = 2\alpha_{q,d} v'_{in,d}[n] + e_{q,d}[n]$.

The total differential mode input to the DCMR flash ADC is $v'_{in,d}[n] = v_{in,d}[n] + w_d[n]$, where $v_{in,d}[n]$ is the desired differential signal and $w_d[n]$ is a dither sequence. Let $v_{in,d}[n]$ be a deterministic, periodic signal with period N. Let $w_d[n]$ be a sequence of independent identically distributed (i.i.d.) random variables with a uniform probability density function (pdf) on $(-\frac{\Delta_d}{2}, \frac{\Delta_d}{2})$. The inputs to the single-ended flash ADCs are then,

$v'_{in+}[n] = \frac{v_{in,d}[n]}{2} + w[n] + v_{cm}[n]$, and $v'_{in-}[n] = -\frac{v_{in,d}[n]}{2} - w[n] + v_{cm}[n]$, where $w[n] = \frac{w_d[n]}{2}$ has a uniform pdf on $(-\frac{\Delta}{2}, \frac{\Delta}{2})$. Because $w[n]$ is uniform dither over the single-ended quantization step, the dither provided on the differential input is sufficient to dither the single-ended flash ADCs and ensure that e_{q+} and e_{q-} are i.i.d. sequences of uniform random variables on $(-\frac{1}{2}, \frac{1}{2})$ independent of $v_{in,d}$ and v_{cm} [3].

The DCMR flash ADC output is $y_d[n] = 2\alpha_{q,d} v_{in,d}[n] + 2\alpha_{q,d} w_d[n] + e_{q,d}[n]$, and expanding $R_{y_d y_d}$ gives,

$$\begin{aligned} R_{y_d y_d} &= 4\alpha_{q,d}^2 R_{v_{in,d} v_{in,d}} + 4\alpha_{q,d}^2 R_{w_d w_d} \\ &+ 2\alpha_{q,d} R_{w_d e_{q,d}} + 2\alpha_{q,d} R_{e_{q,d} w_d} + R_{e_{q,d} e_{q,d}}, \end{aligned} \quad (1)$$

where the n and m arguments of each term have been suppressed for brevity. Because $e_{q+}[n]$, $e_{q-}[n]$ and $w_d[n]$ are zero mean and are independent of $v_{in,d}[n]$, their cross correlations with $v_{in,d}[n]$ are zero and do not appear in (1).

For $m \neq 0$, (1) can be simplified as follows. Because w_d is i.i.d. and zero mean, the $R_{w_d w_d}$ term is zero. Note that $e_{q,d}[n]$ is a memoryless function of the quantizers' inputs at time n and does not depend on inputs at time $m \neq n$. Thus the $R_{w_d e_{q,d}}$, $R_{e_{q,d} w_d}$ and $R_{e_{q,d} e_{q,d}}$ terms can be expressed as the product of expected values, and the fact that $w_d[n]$, $e_{q+}[n]$ and $e_{q-}[n]$ are zero mean implies that these terms are zero. Therefore, (1) can be expressed for all m as

$$R_{y_d y_d}[n,m] = 4\alpha_{q,d}^2 R_{v_{in,d} v_{in,d}}[n,m] + \delta[m]\sigma^2[n], \quad (2)$$

where $\delta[m] = 1$ if $m = 0$ and is zero otherwise, and

$$\sigma^2[n] = 4\alpha_{q,d}^2 \,\mathrm{E}(w_d^2) + 4\alpha_{q,d} \,\mathrm{E}(w_d e_{q,d}[n]) + \mathrm{E}(e_{q,d}^2). \quad (3)$$

From equation (2), it follows that the $S_{y_d y_d}(\omega)$ will be the PSD of $2\alpha_{q,d} v_{in,d}[n]$ plus white noise. Thus provided that the common mode noise does not overload the single-ended ADCs, the DCMR flash ADC rejects arbitrary common mode noise and produces no spurious tones.

The white noise power for $v_{cm} = 0$ can be calculated by noting from Fig. 7a and Fig. 7b that $e_{q-} = -e_{q+}$. Thus, $e_{q,d} = 2e_{q+}$ and $e_{q,d}$ is an i.i.d. sequence of uniform random variables on $(-1, 1)$ and $\mathrm{E}(e_{q,d}^2) = \frac{4}{12}$. This implies that (2) can be written as

$$\begin{aligned} R_{y_d y_d}[n,m] &= 4\alpha_{q,d}^2 R_{v_{in,d} v_{in,d}}[n,m] \\ &+ 4\delta[m] \left(\alpha_{q,d}^2 \,\mathrm{E}(w_d^2) + 2\alpha_{q,d} \,\mathrm{E}(w_d e_{q+}[n]) + \frac{1}{12} \right). \end{aligned}$$

It can be verified that this is four times the result for a conventional $(L+1)$-level flash ADC with input $v_{in,d}[n]$, dither $w_d[n]$ and quantization step size Δ_d. Therefore as asserted above, the DCMR flash ADC is exactly equivalent to a conventional flash ADC followed by a gain of two.

For $v_{cm} \neq 0$, the common mode noise will modulate the white noise power. Note that for $v_{cm} = \frac{\Delta}{4}$ as shown in Fig. 8c, the quantization error will be equivalent to that of a $(2L+1)$-level quantizer and $\mathrm{E}(e_{q,d}^2)$ will be reduced to $\frac{1}{12}$. Thus, the correlation between e_{q+} and e_{q-} offers the potential to realize an equivalent $(2L+1)$-level DCMR flash ADC from a pair of $(L+1)$-level flash ADCs.

Because common mode noise at the input of the DCMR flash ADC will cause $y_d[n]$ to take on even and odd values, dropping the LSB to eliminate the gain of two will result in truncation error correlated to the signal and will give rise to spurious tones in the output as shown in Fig. 4b. However, by using an approach similar that used in a tree-structured mismatch shaping DAC, this requantization error can be made to appear as white noise or spectrally shaped white noise. To illustrate the case where the requanzation noise is whitened, let $r[n]$ be an i.i.d. random bit sequence independent of $v_{in,d}$, v_{cm} and w taking values $+1$ and -1 with equal probability. A switching sequence, $s[n]$, is then generated such that

$$s[n] = \begin{cases} 0, & \text{if } y_d[n] \text{ is even,} \\ \pm 1, & \text{if } y_d[n] \text{ is odd.} \end{cases} \quad (4)$$

Letting $y_d^{(0)}[n]$ denote the LSB of $y_d[n]$, $s[n] = y_d^{(0)}[n] r[n]$. The requantized output is then, $y[n] = \frac{1}{2}(y_d[n] + s[n])$. Because $r[n]$ is independent from $y_d[n]$ and has zero mean, $\mathrm{E}(y_d[n] s[n+m]) = 0$ and $\mathrm{E}(s[n] s[n+m]) = 0$, $m \neq 0$. These results, along with (2), imply $R_{yy}[n,m] = \frac{1}{4} R_{y_d y_d}[n,m] + \frac{1}{4}\delta[m] \,\mathrm{E}(s^2[n])$. Thus both the quantization noise and requantization error appear as white noise in $y[n]$.

The requantization error can be made to appear as white noise shaped by a $(1 - z^{-1})$ filter by letting $s[n]$ be a dithered, first order shaped sequence obeying (4). The circuit shown in Fig. 2 that generates such a sequence is identical to the switching block sequence generator in the $\Delta\Sigma$ modulator's mismatch shaping DAC [4]. This circuit was used rather than whitening the requantization error with a random sequence because it required little additional hardware and offered improved performance.

IV. ACKNOWLEDGEMENT

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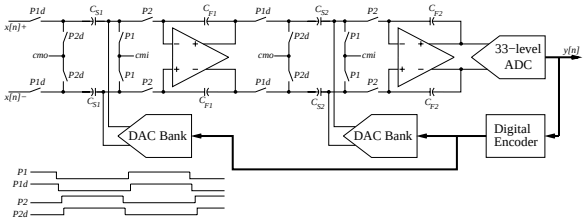

Figure 1: High-level circuit topology of the $\Delta\Sigma$ modulator IC.

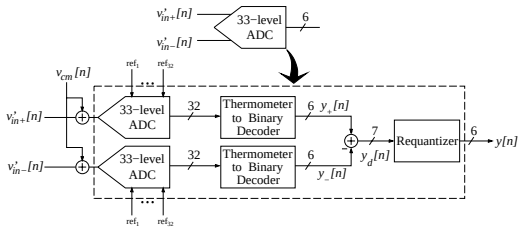

Figure 2: The DCMR flash ADC used in the $\Delta\Sigma$ modulator IC.

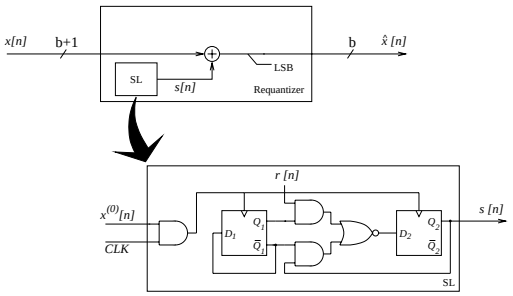

Figure 3: High-level view of the requantizer and the hardware implementation of the switching logic used in the $\Delta\Sigma$ modulator IC.

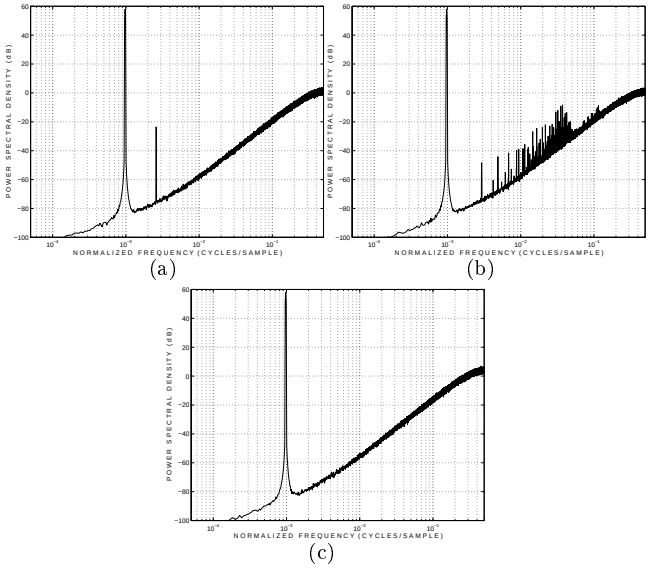

Figure 4: Simulated $\Delta\Sigma$ modulator performance with -6dB, 3kHz input signal and 150mV, 8kHz common mode noise: (a) no common mode rejection, (b) DCMR with truncation and (c) DCMR with shaped requantization.

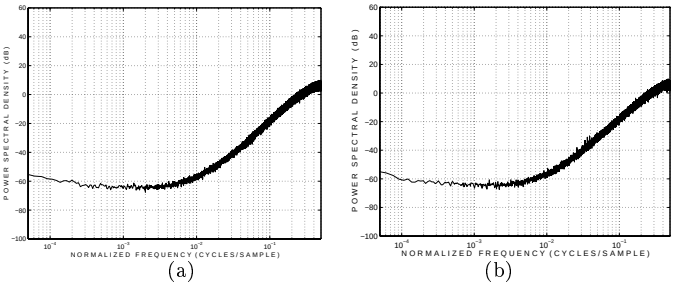

Figure 5: Measured $\Delta\Sigma$ modulator IC performance with dc input: (a) no common mode noise, (b) 150mV peak 8kHz sinusoid on flash ADC reference ladder.

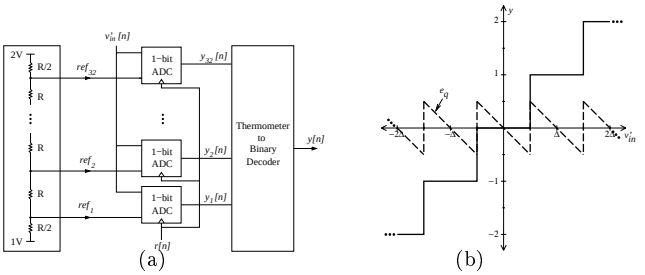

Figure 6: (a) Single-ended flash ADC used in DCMR flash ADC. (b) Flash ADC's transfer function.

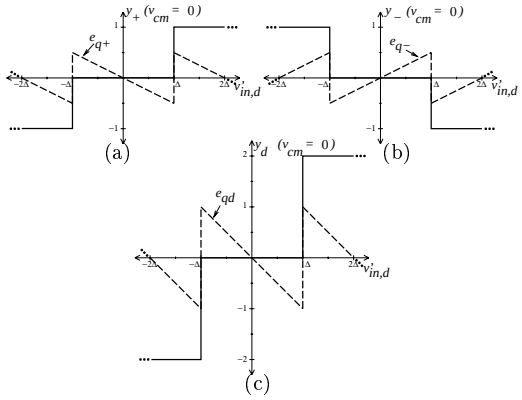

Figure 7: DCMR flash ADC with $v_{cm} = 0$: (a) y_+, e_{q_+} (b) y_-, $e_{q\_}$, (c) y_d, $e_{q,d}$.

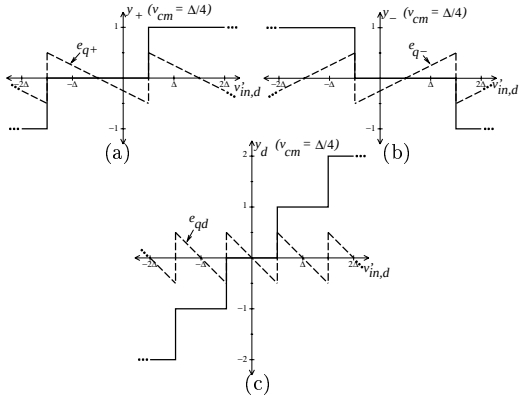

Figure 8: DCMR flash ADC with $v_{cm} = \Delta/4$: (a) y_+, e_{q_+} (b) y_-, $e_{q\_}$, (c) y_d, $e_{q,d}$.

