A DYNAMIC ELEMENT MATCHING TECHNIQUE FOR REDUCED-DISTORTION MULTIBIT QUANTIZATION IN DELTA-SIGMA ADCS

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ABSTRACT

A dynamic element matching (DEM) technique to mitigate the distortion caused by comparator offsets in the flash ADC of a $\Delta\Sigma$ modulator is presented. Measurement results for a high-performance $\Delta\Sigma$ modulator IC using comparator offset DEM are shown to demonstrate the significant reduction in offset-related spurious tones the technique provides. Analysis and simulation of comparator offset DEM in a flash ADC with a periodic input and uniform dither are presented to give insight into its operation and to quantify the spur attenuation it provides.

I. INTRODUCTION

The development of mismatch-shaping multibit DACs has helped to make the implementation of high-performance multibit $\Delta\Sigma$ADCs feasible. Compared to a single-bit design, a multibit $\Delta\Sigma$ modulator using a mismatch-shaping feedback DAC can achieve the same signal to quantization noise specifications with a lower order modulator and reduced oversampling ratio (OSR). In addition, the use of multibit feedback relaxes the slew rate and settling time requirements on the analog integrators. While easing the design of the analog front end, reducing the modulator order and OSR also reduces attenuation of circuit errors in the quantizer. These errors give rise to spurious tones that can limit the signal to noise and distortion (SINAD) and spurious free dynamic range (SFDR) performance of the $\Delta\Sigma$ADC.

When the quantizer is implemented as a flash ADC, quantization level errors stem from resistor ladder reference errors and comparator input offsets. Reference ladder errors result from resistor mismatches and scale with the ladder's reference voltages. In contrast, CMOS comparator input offsets are dominated by the process's inherent threshold voltage mismatches and become increasingly problematic as signal swings are reduced or as the number of quantization levels is increased. In the minimum-size devices required for small-area, high-speed comparators, input offsets with standard deviations on the order of 10mV are typical. While switched-capacitor offset calibration is a simple and effective way of canceling input offsets, this approach significantly increases die area when a large number of comparators are required and large area metal-metal capacitors are the only available linear capacitor structures.

The technique presented in this paper mitigates the distortion introduced by comparator offsets by modulating the sign of each offset with a random bit sequence. This approach, named *comparator offset DEM* because of its similarity to dynamic element matching (DEM) techniques used in DACs, was applied to overcome circuit challenges encountered in the design of a high performance multibit ADC $\Delta\Sigma$ modulator[1]. Because of the choice of architecture and the process limitations, comparator offsets proved to be a barrier to meeting the $\Delta\Sigma$ modulator's 98dB SINAD and 105dB SFDR targets. Comparator offset DEM provided a solution to this problem that avoided the use of metal-metal capacitors and enabled the $\Delta\Sigma$ modulator to meet these aggressive specifications.

II. IMPLEMENTATION IN $\Delta\Sigma$ MODULATOR

The $\Delta\Sigma$ modulator mentioned above is a second order design operating at 3.072MHz with an OSR of 64. Fabricated in a 3.3V, 0.5μm single-poly, triple-metal CMOS process, it achieves 98dB peak SINAD and 105dB SFDR [1]. As shown in Fig. 1, it was implemented with two delaying switched-capacitor integrators, a 33-level mismatch-shaping DAC and a 33-level quantizer. The differential input quantizer was realized using a pair of single-ended 33-level flash ADCs and digital rejection of common mode noise [2].

Because of the signal scaling required for the switched-capacitor integrators, comparator offsets in the flash ADCs presented a barrier to meeting the performance targets. The input range of the flash ADCs was set by the integrators' 1.5V $\pm$ 0.5V single-ended output swing. Thus, the ADCs' nominal step size, Δ, is 31.25mV and their reference levels, ref_k range from $1.0\text{V}+\frac{\Delta}{2}$ to $2.0\text{V}-\frac{\Delta}{2}$. Assuming Gaussian-distributed offsets with a standard deviation, $\sigma_{V_{os}}$ of 10mV, 30% of the comparators are likely to have input offsets greater than 32% of Δ in magnitude. Behavioral simulations of the $\Delta\Sigma$ modulator indicated that the attenuation provided by the noise transfer function — 52dB at the 24kHz passband edge — was not sufficient to guarantee meeting the 105dB SFDR target.

The comparator offset DEM circuitry was added to the $\Delta\Sigma$ modulator with minimal increase in die size. It occupies only 1.5% of the total chip area and requires 65% less area per comparator than the switched-capacitor approach considered for the design. As shown in Fig. 2b, four minimum size transmission gates at the input and output of each comparator were required to implement the switching. The pseudo-random bit sequence was provided by the $\Delta\Sigma$ modulator's existing sequence generator and required no additional area.

Measured results show that comparator offset DEM provides a significant reduction of spurious tones in the $\Delta\Sigma$ modulator output. The $\Delta\Sigma$ modulator was tested with a 2.8V peak, 1.5kHz sinusoidal input, and performance with and without DEM was compared by enabling and

disabling the random bit. The $\Delta\Sigma$ modulator output power spectral density (PSD) without DEM is shown in Fig. 3a, and the PSD with DEM is shown in Fig. 3b. Note that low-frequency odd harmonic distortion — more than 106dB below the input signal — is limited by the performance of the switched-capacitor integrators and is the same in both plots. The harmonic distortion above 15kHz is dominated by the flash ADC comparator offsets, and it can be seen in Fig. 3b that comparator offset DEM provides better than 10dB of attenuation of these harmonics.

To compare the measured performance to that predicted by simulations, the results of behavioral simulations of the $\Delta\Sigma$ modulator are shown in Fig. 4a and Fig. 4b. The simulations used Gaussian-distributed comparator offsets with a standard deviation, $\sigma_{V_{os}}$, of 10mV and Gaussian-distributed DAC mismatch errors with a standard deviation, σ_{DAC}, of 0.33%. In Fig. 4a where comparator offset DEM is disabled, the low-level spurs generated by the comparator offsets are clearly visible over the entire passband. As shown in Fig. 4b, comparator offset DEM attenuates these spurs over the entire signal band.

III. SIGNAL PROCESSING DETAILS

Unlike DAC dynamic element matching techniques that fully whiten mismatch errors for arbitrary input signals, comparator offset DEM requires an input with a random component to achieve a significant reduction in spurious tones. This random component is necessary to make both of each threshold's modulated values affect the output with nearly equal probability. When the flash ADC is used within a multibit $\Delta\Sigma$ modulator having an arbitrarily small amount of input-referred noise, the quantization noise present at the flash ADC's input provides this randomness [3]. To characterize the performance of comparator offset DEM, a nonideal flash ADC with a deterministic input, $v_{in}[n]$, plus uniform dither, $w[n]$ is analyzed. To determine how the offset errors affect the output PSD, $S_{yy}(\omega)$, the autocorrelation sequence, $R_{yy}[n,m] = \mathrm{E}(y[n]y[n+m])$, is computed. It is then shown that for periodic $v_{in}[n]$, $y[n]$ is cyclostationary. The autocorrelation is then used to determine the form of $S_{yy}(\omega)$. It is shown that for a class of inputs, comparator offset DEM causes the offset errors to appear in $S_{yy}(\omega)$ as white noise with no spurious components.

An $(L+1)$-level flash ADC of the form shown in Fig. 2a is considered. The ideal resistor ladder is driven with reference voltages $+V_{ref}$ and $-V_{ref}$ giving a quantization step size, Δ, of $\frac{2V_{ref}}{L}$. The resistor ladder provides L ideal reference levels, denoted $ref_k = k\Delta - \frac{L+1}{2}\Delta$, $k = 1, 2, \ldots L$. Each of the L comparators has a static input offset V_{osk}, $k = 1, 2, \ldots L$. The flash ADC output, $y[n]$, is formed by summing the $y_k[n]$ outputs for $k = 1, 2 \ldots L$ and adding an offset of $-\frac{L}{2}$. Thus, $y[n]$ takes on values from $\{-\frac{L}{2}, -\frac{L}{2}+1, \ldots \frac{L}{2}\}$ and can be viewed as a gain element with gain $\alpha_q = \frac{1}{\Delta}$ followed by an additive error source, $e_q[n]$.

The effect of positive and negative offsets on the flash ADC's transfer function at threshold ref_k is shown in Fig. 5a. The quantization error, e_q, is shown in Fig. 5b with the quantization error of an ideal flash ADC, e_q^i, indicated by the dashed line. The component of e_q due to threshold error, e_q^t, is shown in Fig. 5c. Thus, the total quantization error, $e_q[n]$ can be represented as $e_q^i[n] + e_q^t[n]$.

The flash ADC's input is $v'_{in}[n] = v_{in}[n] + w[n]$, where $v_{in}[n]$ is a deterministic, periodic input signal with period N and $w[n]$ is a sequence of independent, identically distributed (i.i.d.) uniform random variables on $(-\frac{\Delta}{2}, \frac{\Delta}{2})$. Let $f_w(w)$ denote the probability density function (pdf) of w. The quantizer output is then, $y[n] = \alpha_q v_{in}[n] + \alpha_q w[n] + e_q^i[n] + e_q^t[n]$. Uniform i.i.d. dither ensures that $e_q^i[n]$ is an i.i.d. sequence of uniform random variables on $(-\frac{1}{2}, \frac{1}{2})$ [4].

Expanding $R_{yy}[n,m]$ into its component terms yields

$$\begin{aligned} R_{yy}[n,m] &= \alpha_q^2 R_{v_{in}v_{in}} + \alpha_q R_{v_{in}e_q^t} + \alpha_q R_{e_q^t v_{in}} \\ &+ R_{e_q^t e_q^t} + R_{e_q^i e_q^t} + R_{e_q^t e_q^i} + \alpha_q R_{we_q^i} + \alpha_q R_{e_q^i w} \\ &+ \alpha_q R_{we_q^t} + \alpha_q R_{e_q^t w} + \alpha_q^2 R_{ww} + R_{e_q^i e_q^i}, \end{aligned} \tag{1}$$

where the n and m arguments of each term are suppressed for brevity. The $R_{v_{in}w}$, $R_{wv_{in}}$, $R_{v_{in}e_q^i}$ and $R_{e_q^i v_{in}}$ terms are zero because e_q^i and w are independent of v_{in} and have zero mean.

Because w and e_q^i are i.i.d. and zero mean and because $e_q^t[n]$ and $e_q^i[n]$ are memoryless functions of the quantizer input at time n, (1) can be simplified to

$$R_{yy}[n,m] = R'_{yy}[n,m] + \delta[m]\sigma^2[n], \tag{2}$$

where $\delta[m] = 1$ for $m = 0$ and is zero otherwise, and where

$$\begin{aligned} R'_{yy}[n,m] &= \alpha_q^2 R_{v_{in}v_{in}} + \alpha_q v_{in}[n]\,\mathrm{E}\big(e_q^t[n+m]\big) \\ &+ \alpha_q v_{in}[n+m]\,\mathrm{E}\big(e_q^t[n]\big) + \mathrm{E}\big(e_q^t[n]\big)\,\mathrm{E}\big(e_q^t[n+m]\big), \end{aligned} \tag{3}$$

and

$$\begin{aligned} \sigma^2[n] &= \mathrm{E}\Big(e_q^t[n]^2\Big) - \mathrm{E}\big(e_q^t[n]\big)^2 \\ &+ \Big(R_{e_q^i e_q^t} + R_{e_q^t e_q^i}\Big) + \alpha_q\Big(R_{we_q^i} + R_{e_q^i w}\Big) \\ &+ \alpha_q\Big(R_{we_q^t} + R_{e_q^t w}\Big) + \alpha_q^2 R_{ww} + R_{e_q^i e_q^i}. \end{aligned} \tag{4}$$

Note that $R'_{yy}[n,m]$ contains all the terms of (1) that are nonzero for $m \neq 0$ and that the correlation terms in $\sigma^2[n]$ are evaluated at $[n,0]$.

Because, $w[n]$ is i.i.d. and because the pdf of $v'_{in}[n]$, $f_{v'_{in}[n]}(x)$, is equal to $f_w(x - v_{in})$, it can be shown that $\sigma^2[n]$ is periodic in n with period N and $R'_{yy}[n,m]$ is periodic in both indices with period N. With these results, it follows that for all m, (2) is periodic in n with period N. This implies that $y[n]$ is cyclostationary and

$$\tilde{R}_{yy}[m] = \tilde{R}'_{yy}[m] + \tilde{\sigma}^2\delta[m], \tag{5}$$

where

$$\tilde{R}'_{yy}[m] = \frac{1}{N}\sum_{n=0}^{N-1} R'_{yy}[n,m], \qquad \tilde{\sigma}^2 = \frac{1}{N}\sum_{n=0}^{N-1}\sigma^2[n].$$

Because (5) consists of a $\delta[m]$ term plus terms that are periodic in m, it follows that its PSD — the Fourier transform of $\tilde{R}_{yy}$ — consists of the signal, white noise with power $\tilde{\sigma}^2$ and spurious tones determined by the e_q^t-dependent terms of $\tilde{R}'_{yy}[m]$.

Using (5), the PSD can be computed given a set of V_{os} errors and an input $v_{in}[n]$ by evaluating

$$\mathrm{E}\left(e_q^t\right) = \int_{-\infty}^{\infty} e_q^t(x) f_w(x - v_{in})\mathrm{d}x \qquad (6)$$

for each sample of the periodic input $v_{in}[n]$. This expression can be considered an "average error transfer function" giving an output sample, $\mathrm{E}\left(e_q^t[n]\right)$, for each input sample, $v_{in}[n]$. Because (6) is in the form of a convolution integral, this error transfer function can be computed by graphically evaluating $e_q^t * f_w$.

Flash ADC Without Comparator Offset DEM

The transfer function e_q and its threshold component, e_q^t, are shown in Fig. 6a and Fig. 6b for a nonideal flash ADC without comparator offset DEM. The transfer function $\mathrm{E}\left(e_q^t\right)$ shown in Fig. 6c has been computed by graphically evaluating $e_q^t * f_w$. Note that for $V_{osk} \neq 0$, $\mathrm{E}\left(e_q^t\right)$ is nonzero for all v_{in} except the points where $\mathrm{E}\left(e_q^t\right)$ changes sign. Thus for almost all signals of interest, the sequence $\mathrm{E}\left(e_q^t[n]\right)$ will be nonzero. It follows that the e_q^t-dependent terms of $\tilde{R}'_{yy}$ are nonzero and $S_{yy}(\omega)$ will have spurious components.

Flash ADC With Comparator Offset DEM

By performing the switching shown in Fig. 2b, the block labeled *1-bit ADC* behaves as a comparator whose input offset voltage is modulated by an i.i.d. random bit sequence, $r[n]$. The comparator output is then $y_k[n] = 1$ if $v_{in}[n] > ref_k \pm V_{os}$ and $y_k[n] = 0$ otherwise, where the sign of the offset is positive for $r[n] = 1$ and negative for $r[n] = 0$. The error transfer functions e_q and e_q^t for each state of r are shown in Fig. 7a and Fig. 7b. Since $r[n]$ and $w[n]$ are independent, e_q^t can be averaged first over the states of r to derive the transfer function shown in Fig. 7c.

From $\mathrm{E}\left(e_q^t\right)$ shown in Fig. 7d, it can be seen that the key benefit provided by comparator offset DEM is the creation of large zero regions in the $\mathrm{E}\left(e_q^t\right)$ transfer function by producing equal area positive and negative error regions in e_q^t centered at each threshold. When f_w is convolved with e_q^t as shown in Fig. 7c, the positive and negative errors cancel each other for much of the flash ADC's input range. The regions where $\mathrm{E}\left(e_q^t\right) = 0$ correspond to those input values where the dither pdf "covers" both the positive and negative error regions giving equal probability of positive and negative threshold-induced quantization error. The nonzero regions centered between the quantizer thresholds correspond to input values where the dither pdf does not cover both error regions equally and the probabilities of positive and negative errors are unequal.

An input $v_{in}[n]$ that completely avoids the nonzero regions of $\mathrm{E}\left(e_q^t\right)$ will have $\mathrm{E}\left(e_q^t[n]\right) = 0$ and $\tilde{R}'_{yy}[m] = \alpha_q^2 \tilde{R}'_{v_{in}v_{in}}[m]$. Thus, $S_{yy}(\omega)$, will consist only of the signal and white noise without spurious components. For an input with some samples in the nonzero regions of $\mathrm{E}\left(e_q^t\right)$, the offset errors will give rise to both white noise and attenuated spurious components in $S_{yy}(\omega)$. Simulation results for a wide range of inputs indicate that comparator offset DEM still provides significant spur attenuation in this case.

Simulation Example

To illustrate the partial and full spur attenuation predicted by the analysis, Fig. 8 and Fig. 9 show simulation results for a five-level flash ADC with random errors $|V_{osk}| < \frac{\Delta}{8}$ and uniform i.i.d. dither $w[n]$. In Fig. 8, the input signal was chosen to be $v_{in}[n] = \Delta \sin(\frac{\pi}{4}n)$ to force half of its samples to land in the mid-threshold regions where $\mathrm{E}\left(e_q^t\right) \neq 0$. Without comparator offset DEM, as shown in Fig. 8a, the flash ADC has an SFDR of 24.4dB. With DEM enabled as shown in Fig. 8b, the third harmonic is reduced significantly, but the SFDR is limited to 26.5dB by the second harmonic. The results with an input $v_{in}[n] = \Delta \sin(\frac{\pi}{4}n) + \frac{\Delta}{8}$ are shown in Fig. 9. This choice of input forces every sample to land in a region where $\mathrm{E}\left(e_q^t\right) = 0$. The results without DEM shown in Fig. 9a indicate that the flash ADC has an SFDR of 30.5dB. The PSD in Fig. 9b shows that with DEM enabled, no spurs are visible in the output and the SFDR is improved to better than 45dB. As predicted, comparator offset DEM completely whitens the comparator offset errors for this input signal.

IV. ACKNOWLEDGMENT

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V. REFERENCES

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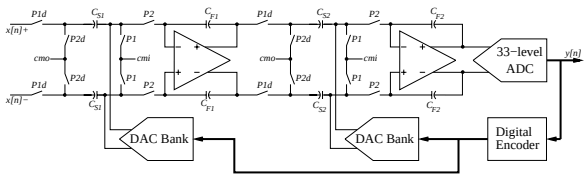

Fig. 1: $\Delta\Sigma$ modulator circuit topology.

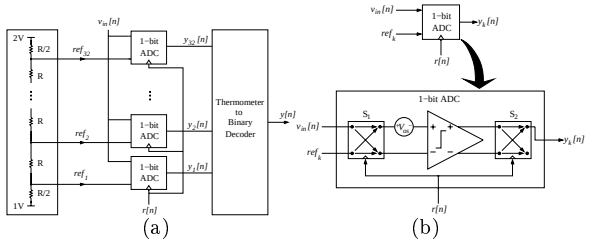

Fig. 2: (a) Flash ADC toplogy. (b) Comparator offset DEM.

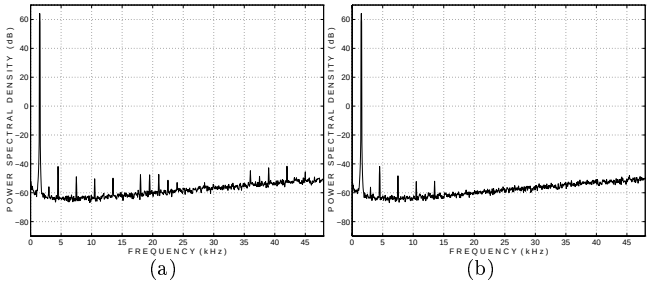

Fig. 3: Measured $\Delta\Sigma$ modulator results: (a) DEM off, (b) DEM on.

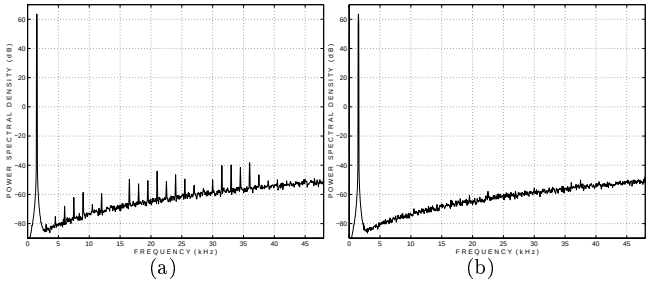

Fig. 4: Simulated $\Delta\Sigma$ modulator results: (a) DEM off, (b) DEM on.

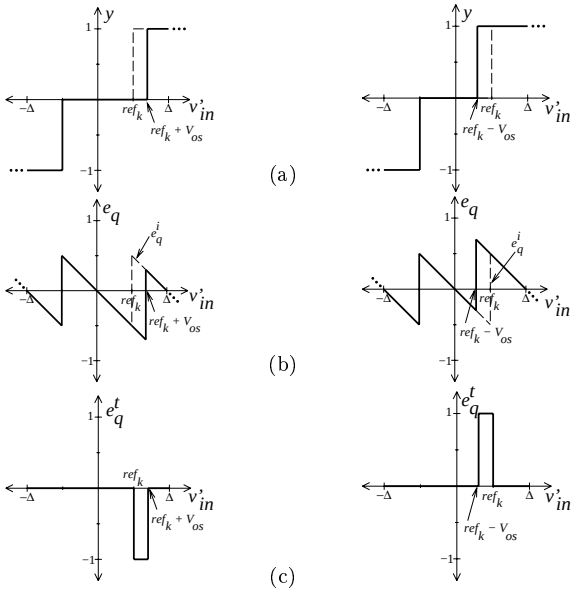

Fig. 5: Behavior at ref_k for $\pm V_{os}$: (a) ADC output, (b) quantization error, (c) threshold error.

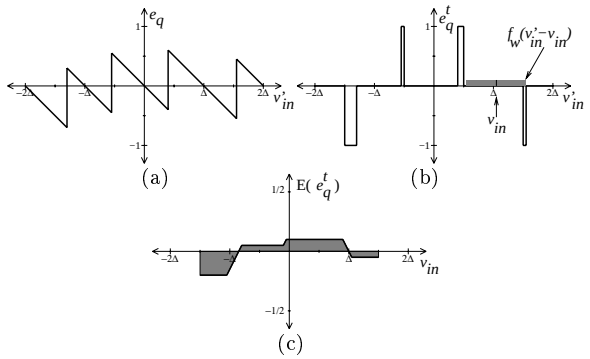

Fig. 6: Flash ADC without DEM: (a) $e_q(v'_{in})$, (b) $e_q^t(v'_{in})$, (c) $\mathrm{E}(e_q^t)$.

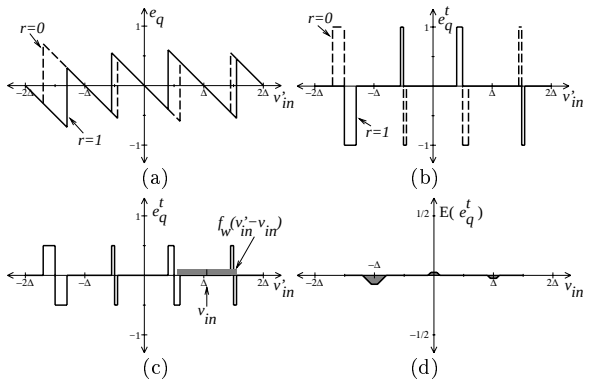

Fig. 7: Nonideal flash ADC with DEM: (a) $e_q(v'_{in})$, (b) $e_q^t(v'_{in})$, (c) $e_q^t(v'_{in})$ averaged over r, (d) $\mathrm{E}(e_q^t)$.

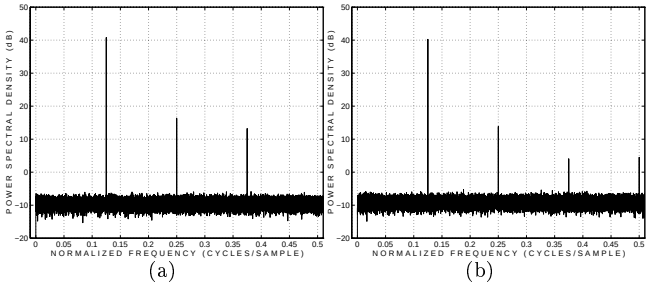

Fig. 8: Flash ADC simulation results, $v_{in}[n]$ in $E(e_q^t) \neq 0$ regions: (a) DEM off, (b) DEM on.

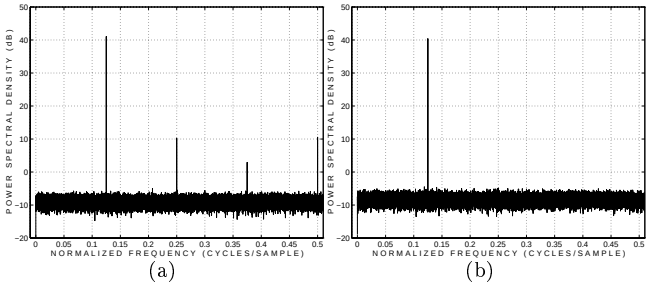

Fig. 9: Flash ADC simulation results, $v_{in}[n]$ in $E(e_q^t) = 0$ regions: (a) DEM off, (b) DEM on.

