A 3.3V Single-Poly CMOS Audio ADC Delta-Sigma Modulator with 98dB Peak SINAD

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Abstract

This paper presents a second-order $\Delta\Sigma$ modulator for audio-band A/D conversion implemented in a 3.3V, 0.5μm, single-poly CMOS process that achieves 98dB peak SINAD and over 100dB SFDR. The design uses a reduced-complexity, mismatch-shaping 33-level DAC and a 33-level flash ADC with digital common-mode rejection and dynamic element matching of comparator offsets. These signal processing innovations, combined with established circuit techniques, enable state of the art performance in CMOS optimized for digital circuits. To the knowledge of the authors, this level of performance has not been achieved previously under these process constraints [1], [2], [3].

Introduction

The availability of CMOS for implementing inexpensive, high-volume digital circuits makes integrating signal processing systems on a single chip attractive in many situations. The types of functions that can be integrated and the scope of integration are often limited by the ability to perform high resolution data conversion in CMOS optimized for digital circuits. An example of such a system is a high-performance audio processing system where 48 kSample/sec A/D conversion with 98dB SINAD and SFDR is required. Integrating such a converter on a 3.3V, single-poly CMOS process requires overcoming process-induced circuit challenges.

Without double-poly or other thin-oxide capacitors, the metal interconnect layers provide the only inherently linear means to implement switched-capacitor circuits. The large bottom plate parasitic capacitance of all-metal capacitors requires high current drive amplifiers. The 3.3V supply limits signal swings necessitating increased sampling capacitances to meet signal to thermal noise requirements. These factors make designing fast-settling, low-distortion integrators a difficult circuit design problem. This paper presents a solution to this problem based on multibit $\Delta\Sigma$ modulation which eases the requirements on the switched-capacitor circuitry.

$\Delta\Sigma$ Modulator

Multibit quantization in the $\Delta\Sigma$ modulator reduces the quantization noise power that must be shaped out of band relative to single-bit architectures. Thus, the order of the modulator loop filter and the oversampling ratio can be reduced. The simpler loop filter reduces the complexity of the switched-capacitor circuitry, and the lower oversampling ratio eases the integrators' settling time requirements. The reduction in quantization error implies that the maximum step taken by the integrators is reduced, further relaxing the settling requirements.

To meet the 98dB SINAD and SFDR targets, the 33-level, second-order $\Delta\Sigma$ modulator shown in Fig. 1 was used [4]. It operates at an oversampling ratio of 64 and samples the 0Hz–24kHz input signal at 3.072MHz. With ideal analog components and no DAC element mismatches, it achieves 108dB peak SINAD. Fig. 2 and Fig. 3 show the switched-capacitor implementations of the $\Delta\Sigma$ modulator and feedback DACs, respectively.

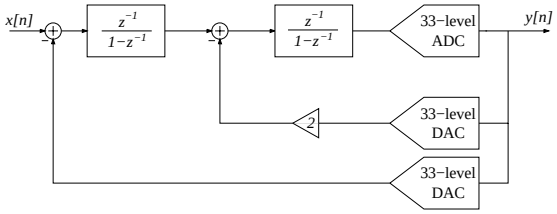

Figure 1: The high-level modulator topology.

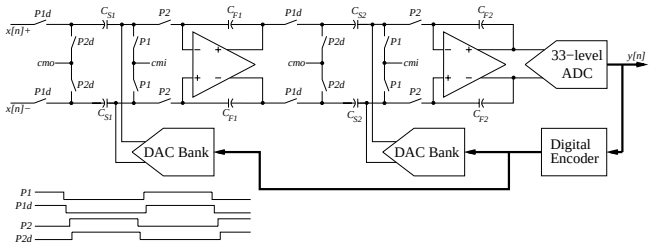

Figure 2: The circuit-level modulator topology.

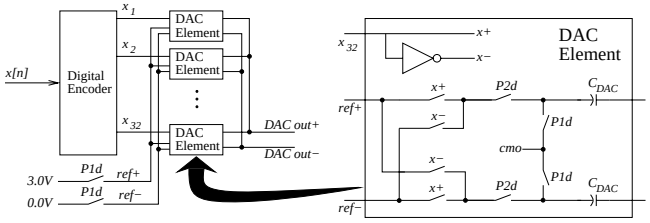

Figure 3: The DAC bank circuit topology.

While the multibit approach eases the switched-capacitor circuit design, it introduces several new problems that must be addressed to meet the performance specifications. The multibit feedback DAC must have the same signal-band precision as the overall converter, since errors introduced by the DAC are not noise-shaped. Error introduced by static DAC element mismatches can be shaped out of band using a digital encoder, but the cost of implementing the encoder must not outweigh the benefits gained in the analog circuit design. To preserve

the common-mode noise rejection of the fully-differential switched-capacitor circuitry, the multibit quantizer must operate on differential input and reference levels. As the number of quantization levels increases, the quantizer step size becomes comparable to the input offset of a CMOS comparator. Though noise-shaped, the errors in a simple flash ADC can become large enough to limit the converter's SFDR.

Signal Processing Details

Reduced-Complexity Mismatch-Shaping DAC

The $\Delta\Sigma$ modulator uses the mismatch-shaping DAC encoder based on [5] shown in Fig. 4 and Fig. 5. In behavioral simulations, the $\Delta\Sigma$ modulator with this digital encoder and with $3\sigma = 1\%$, Gaussian-distributed mismatch errors achieves 104dB peak SINAD.

Each switching block shown in Fig. 4 was implemented as shown in Fig. 5 [6]. This implementation is logically equivalent to that presented in [5] but avoids the need to explicitly implement adders in each switching block through the use of an extra-LSB number representation and logic minimization. To prevent the introduction of spurious tones, each of the five layers of switching blocks is dithered with a single-bit random sequence uncorrelated with those in the other layers.

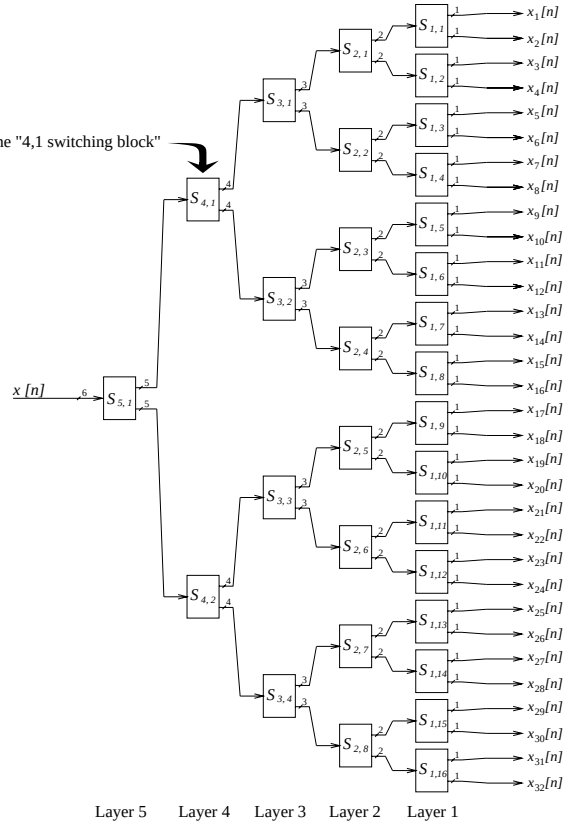

Figure 4: Mismatch-shaping DAC encoder.

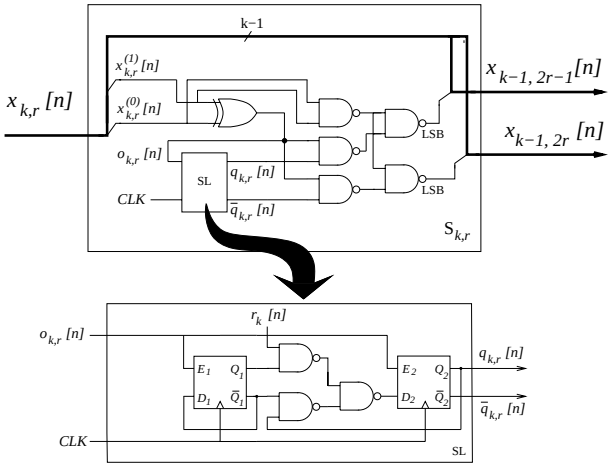

Figure 5: Switching block implementation.

The mismatch-shaping encoder is comprised of 286 logic gates and 90 D flip-flops. Of these, the seven gates and 28 flip-flops required to generate the random bit sequences were implemented off-chip to facilitate experimentation. The pseudo-random sequence generator used for testing produces seven random bit sequences uncorrelated for time shifts less than 12.48 seconds.

Differential Flash ADC

The conventional approach to implementing a multibit quantizer in a $\Delta\Sigma$ modulator is to use switched-capacitors to sample and compare the differential integrator output and differential reference levels [4]. For a 33-level ADC, a bank of 64 capacitors and switches comparable to the area of the DAC array would be required. In addition, buffering the reference ladder with source-followers presents a circuit design challenge given the limited headroom. To avoid these problems, an approach that eliminates the need for switched-capacitors was used.

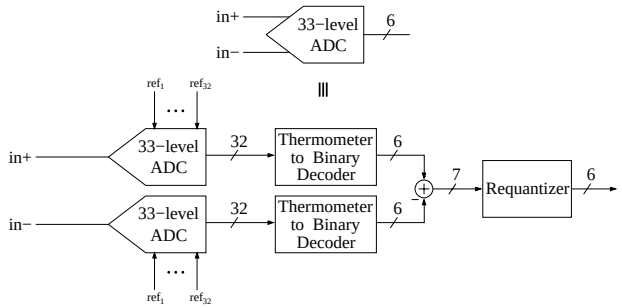

Figure 6: High-level view of the 33-level flash ADC.

The flash ADC architecture, shown in Fig. 6, digitizes the positive and negative differential outputs of the second integrator with a pair of single-ended, 33-level flash ADCs. The thermometer-coded outputs are passed through a bubble-detection circuit, converted to binary

and subtracted. The differencing operation preserves the differential-mode signal and cancels the common-mode noise. However, the result is a 65-level value that must be requantized to 33-levels for the mismatch-shaping DAC encoder.

In the absence of common-mode noise, the difference would always be an even number, and the LSB could be truncated without introducing any error. However, common-mode noise can generate odd values. In such cases, if the signal were truncated, the resulting requantization noise would degrade the SFDR. To avoid this problem, the requantization is controlled by a dithered, first-order switching block identical to that used in the mismatch-shaping DAC encoder. The switching block causes odd values to be rounded up or down such that the requantization error is first-order noise-shaped.

Relative to a single differential input ADC, the digital common-mode rejection architecture requires two single-ended, 33-level flash ADCs, a second debubbling circuit and thermometer-to-binary encoder, a 6-bit subtractor, a 5-bit adder, a switching block, and a single-bit random sequence. The logic totals 240 logic gates and two D-flip-flops. As shown in the next section, this approach resulted in significant area savings.

Though not implemented in the prototype, a refinement of this design makes use of a pair of 17-level flash ADCs whose reference levels are offset by one-half of one quantization step. After differencing, the 33-level result could be presented directly to the mismatch-shaping DAC encoder without the need for requantization.

Dynamic Element Matching Comparator

Behavioral simulations indicated that comparator offsets on the order of 10mV would limit the SFDR. Comparator offset calibration was ruled out, since 64 comparators are required for the pair of 33-level flash ADCs, and increasing the comparator's complexity could potentially eliminate any net area savings in the digital common-mode rejection architecture. Instead, dynamic element matching is used to spectrally whiten errors caused by comparator input offsets.

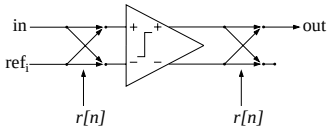

Figure 7: Implementation of the DEM comparator.

Fig. 7 shows the dynamic element matching comparator. The input and output of each comparator in the flash ADC are swapped by a single-bit random sequence. The swapping is performed by transmission gates arranged such that sign of the comparator's offset is modulated by the random sequence but the polarity of the signal is unaffected. Because only one threshold is active in each ADC per sample, the random sequence only affects one comparator in each ADC per sample. Thus, a single sequence is sufficient for the entire ADC.

Circuit Implementation Details

The 3.0V peak differential input voltage and DAC reference voltage were chosen to achieve the 104dB signal to thermal noise target with the smallest possible sampling capacitor. The first integrator uses 4.35pF sampling capacitors and an array of 32 pairs of 136fF DAC capacitors. Because the integrator output must be scaled down to the output swing of the integrator, the 26.9pF feedback capacitor dominates the first integrator loading.

The DAC array is designed to fully charge and discharge 32 capacitors to each reference on each full clock cycle. This prevents signal-dependent reference loading that can generate second harmonic distortion. The switches controlled by $x+$ and $x-$ (Fig. 3) determine whether the DAC element is charged in a positive or negative sense. Four transmission gates are required per DAC element, and they are placed on the bottom plate side to keep the summing nodes of the integrator as small and well-shielded as possible.

Standard switched-capacitor techniques such as delayed bottom plate switching are used. The switches were sized carefully to make the bandwidth just large enough to allow complete settling to reduce susceptibility to digital switching noise and to reduce charge injection.

The integrators use single-stage folded-cascode OTAs with differential gain enhancement [7]. The amplifiers are designed for exponential settling without slew-rate limiting, and the output swing is modest to keep the DC gain relatively constant over the entire output range. Over temperature, supply, loading, process corners and the 1V peak differential output range, simulations show that during P1 the first integrator has $>$ 118dB DC Gain, $>$ 40.5MHz unity gain bandwidth and $>$ 57°phase margin and during P2 it has $>$ 106dB DC Gain, $>$ 13.9MHz unity gain bandwidth and $>$ 112°phase margin.

To verify that incomplete settling does not lead to appreciable distortion, the modulator was simulated in Hspice using full-transistor integrators and behavioral logic for 8192 cycles and the result was analyzed in Matlab. The distortion measured in simulation is more than 100dB below the fundamental.

Prototype Results

Fig. 8 shows the die photograph and Fig. 9 shows the layout floorplan of the prototype $\Delta\Sigma$ modulator. The chip contains 10,747 transistors and measures 5mm by 1.9mm including pads and ESD protection. The floorplan demonstrates that the area is dominated by the metal capacitors. The switched-capacitor circuits were designed conservatively to ensure low distortion and noise; the design could be further refined to scale down the area and power of the second integrator stage.

Reducing analog complexity and capacitor area at the cost of increasing the digital complexity results in net area savings. From the floorplan, it can be seen that the capacitor area required to implement a switched-capacitor differential input flash ADC, roughly equal to the DAC array, is larger than the pair of flash ADCs used

in this design. The additional digital logic to implement the mismatch-shaping DAC, digital common-mode rejection and comparator DEM occupy 14% of the chip area and consume 4% of the total power.

Table 1 summarizes the device specifications and performance. Fig. 10 shows the inband power spectral density for a 2.8V peak, differential input signal at 3.0kHz. Fig. 11 shows the $\Delta\Sigma$ modulator's 3.0kHz SINAD versus input level. Additional single-tone tests were performed for frequencies ranging over the input band and the measured peak SINAD and SFDR were found to be better than 98dB in all cases.

TABLE 1
Performance and Specification Summary

Sample Rate	3.072MHz
Oversampling Ratio	64
Full-scale input range	$\pm$3.0V peak differential
Peak SINAD	98.1dB at 2.8V, 46.88Hz–24.05kHz
SFDR	$>$ 100dB, 46.88Hz–24.05kHz
Power dissipation	66mW analog, 2.6mW digital
Technology	3.3V, 0.5μm CMOS (1 poly, 3 metal)
Chip size	5mm $\times$ 1.9mm
Package	65 pin PGA

The $\Delta\Sigma$ modulator's performance demonstrates that the signal processing innovations used in the design—mismatch-shaping multibit feedback DACs, digital rejection of common-mode noise in the flash ADC, and DEM of comparator offsets—enable the design of high performance ADCs in a single-poly 3.3V CMOS process using well-established switched-capacitor design techniques.

Acknowledgement

This work was supported by the National Science Foundation under Grant MIP-9711331.

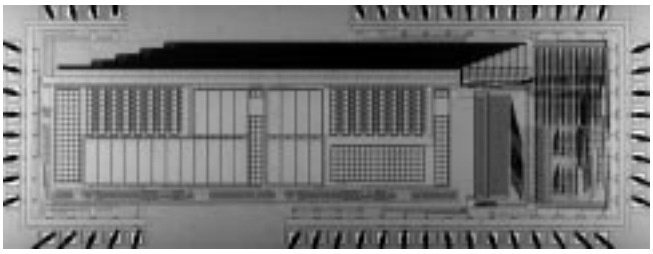

Figure 8: Die photograph.

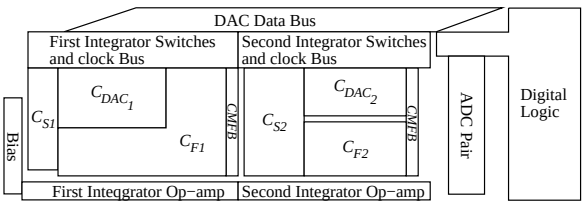

Figure 9: Layout floorplan.

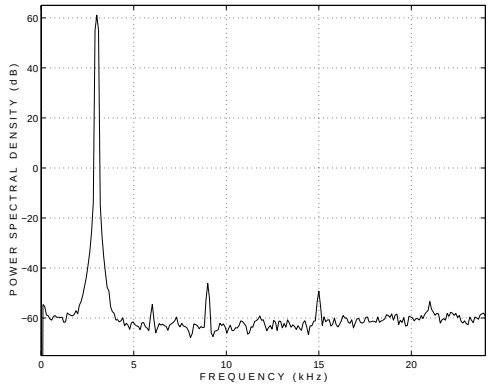

Figure 10: Inband power spectral density; 3.0kHz, -0.5dBFS input.

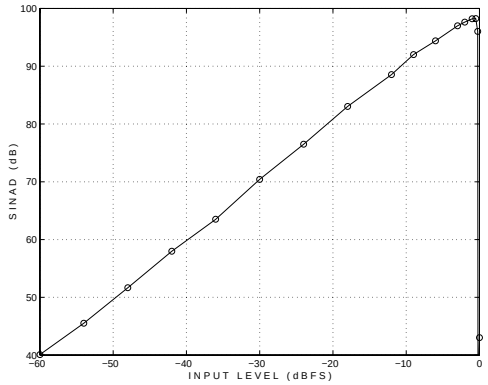

Figure 11: SINAD versus input level.

References

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