An Analysis of the Partial Randomization Dynamic Element Matching Technique

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***Abstract*— Partial randomization dynamic element matching (DEM) was recently introduced as a promising DEM technique for low harmonic distortion digital-to-analog conversion. The DEM technique is well suited for applications such as direct digital synthesis in wireless communication systems for which low hardware complexity is essential in addition to low harmonic distortion. Previously reported simulation results demonstrate that partial randomization DEM greatly attenuates harmonic distortion resulting from static errors in the analog output levels of the DAC, while offering considerable savings in hardware compared to other DEM techniques. This paper presents the first quantitative performance analysis of partial randomization DEM. As a main result, the minimum spurious-free dynamic range provided by the digital-to-analog converter has been quantified as a function of its hardware complexity and the analog output level errors.**

I. Introduction

DIRECT digital synthesis (DDS) has emerged as an efficient and flexible method of generating analog signals of high spectral purity [1]. A key component of a DDS system is the digital-to-analog converter (DAC), which must introduce very little harmonic distortion to honor the spectral purity of the synthesized digital signal. Unfortunately, nonideal circuit behavior in practical DAC's inevitably gives rise to *DAC noise* that consists largely of harmonic distortion and ultimately limits the achievable DDS performance.

Dynamic element matching (DEM) has emerged as a means of mitigating the deleterious effects of nonideal circuit behavior in DAC's by essentially causing a large portion of the DAC noise to be broken into white noise instead of harmonic distortion. Partial randomization DEM was recently introduced as a promising DEM technique for low harmonic distortion DAC's [2]. As will be shown in this paper, the technique offers a trade of spur suppression for hardware complexity.

The partial randomization DEM DAC incorporates a bank of coarse DAC's, referred to as *DAC-elements*, the outputs of which are summed together to yield a composite DAC. Inevitable nonideal circuit behavior results in analog output errors of the DAC elements, giving rise to DAC noise. The DAC noise can be viewed as consisting of two components, namely a component caused by the *static* part of the analog output errors and a component caused by the *dynamic* part of the analog output errors. To the extent that the latter component is below—or can be attenuated to—the maximum allowable level of harmonic distortion for a given DAC application, a good "engineering solution" to mitigate the effects of the static analog output errors is to merely attenuate the resulting harmonic distortion to the maximum level that can be tolerated. Simulations reported in [2] indicate that partial randomization DEM can be used to achieve this result, while offering a significant reduction in hardware complexity over other DEM techniques. However, this finding was supported by simulation results only.

This paper provides a rigorous analysis of the performance of partial randomization DEM. In particular, given a desired minimum spurious-free dynamic range (SFDR) and knowledge of the statistics of the static analog output errors, the analysis can be used to quantify the hardware requirement of the DEM technique for any DAC bit-resolution of interest. As an example, the theoretical results are applied in an IC fabrication yield estimation analysis of the minimum SFDR provided by the 8-bit version of the DAC.

II. Architecture

To review the architecture of the proposed DAC, consider the example 8-bit version shown in Fig. 1. The digital input $x[n]$ is a sequence of unsigned 8-bit numbers less than 256. The DAC consists of three layers of digital devices, each referred to as a *switching block* and collectively referred to as the *digital encoder*, followed by an array of eight *DAC-banks*, each labeled DB_i, and an analog output summing node. The number of layers is referred to as the *randomization index* I, (i.e., $I = 3$ in Fig. 1) and the layers are numbered 6 through 8. Each switching block is labeled $S_{k,r}$, where k denotes the layer number and r denotes the position of the switching block in the layer.

Fig. 2 shows the functional details of the switching block $S_{k,r}$. The switching block has one $k+1$-bit input, two k-bit outputs, and an input for a *random control bit* $c_k[n]$. The random control bit $c_k[n]$ is common to all the switching blocks in the kth layer and is ideally a white random bit-sequence, statistically independent of the random control bits applied to the other layers. When $c_k[n]$ is high, the MSB of the input is mapped to all k bits of the top output, and the remaining k bits of the input are mapped directly to the k bits of the bottom output. When $c_k[n]$ is low, the mappings are interchanged. This process of randomly mapping the input to the outputs is referred to as *random switching*. As indicated in Fig. 1, the

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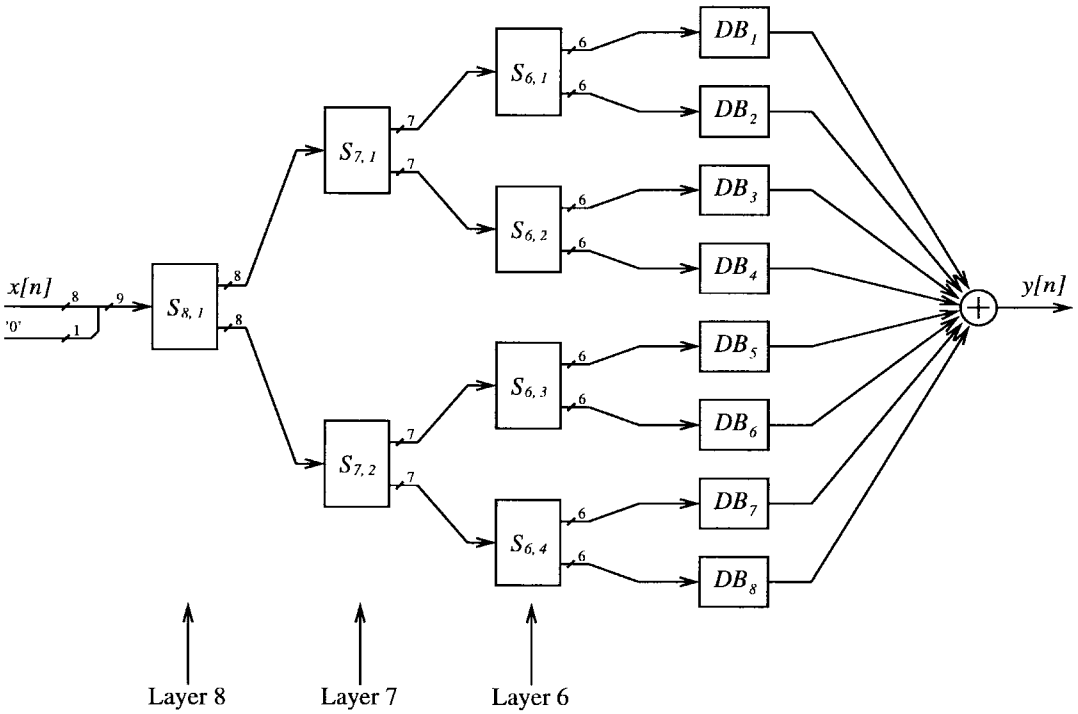


Fig. 1. An 8-bit version of the proposed DAC architecture with randomization index $I = 3$. The layers are numbered 6 through 8.

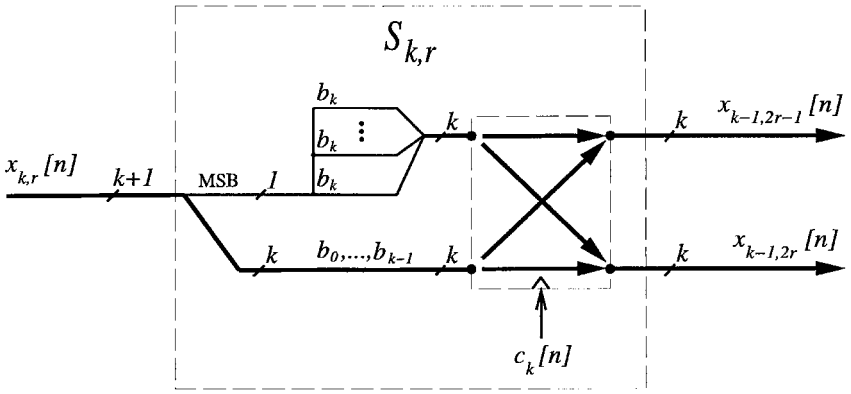


Fig. 2. Details of the switching block of the kth layer.

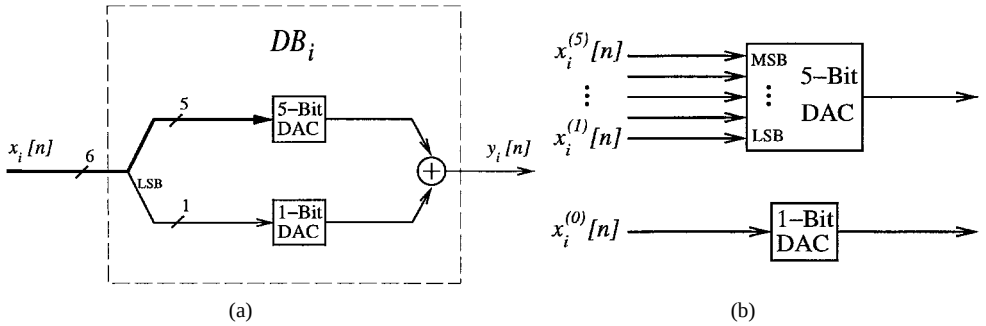


Fig. 3. Details of the DAC bank corresponding to the example 8-bit DAC of Fig. 1. (a) The interconnection of the 5-bit and 1-bit conventional DAC's and (b) the assignment of the input bits.

DAC input $x[n]$ is assigned to the $S_{b,1}$ input bits b_1 through b_b, and a zero is assigned to the input bit b_0.

Fig. 3 shows the functional details of the ith DAC bank. As shown in Fig. 3(a), the DAC bank has a 6-bit input $x_i[n]$ and an analog output $y_i[n]$. It is functionally equivalent to a 5-bit *conventional DAC* and a 1-bit conventional DAC, with $y_i[n]$ formed as the sum of the outputs of the two conventional DAC's. Notice that $x_i[n]$ corresponds to the sequence $x_{5,i}[n]$ with the notation in Fig. 2, where the subscript "5" has been omitted for convenience. The DAC-bank input $x_i[n]$ is

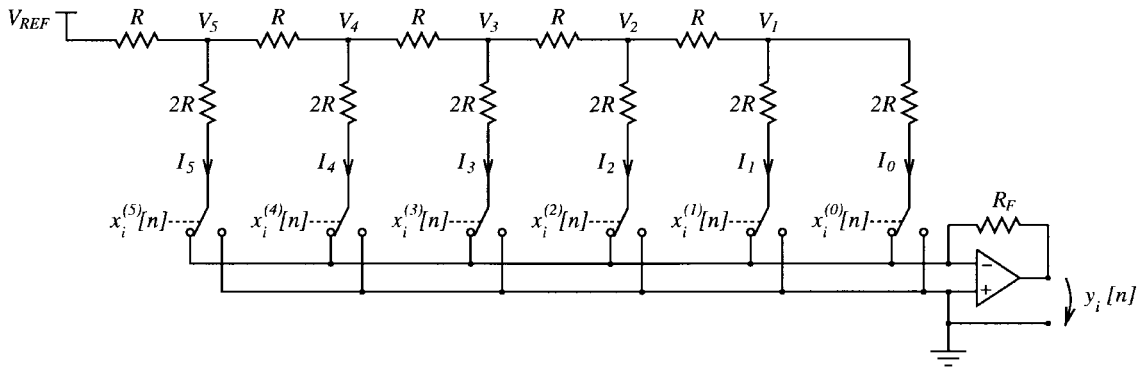


Fig. 4. An implementation of the DAC bank using an (ideal) $R-2R$ ladder network.

interpreted as a sequence of unsigned integers in the range $0, 1, \cdots, 32$, formed as

$$x_i^{(0)}[n] + \sum_{j=1}^{5} 2^{j-1} x_i^{(j)}[n] \tag{1}$$

where $x_i^{(j)}[n]$ denotes the jth bit of $x_i[n]$. As shown in Fig. 3(b), the input to the 5-bit conventional DAC consists of the five MSB's of $x_i[n]$ and is interpreted as a sequence of unsigned integers in the range $0, 1, \cdots, 31$. The input to the 1-bit conventional DAC is the LSB of $x_i[n]$ and is interpreted as a sequence of numbers that are either zero or one.

Fig. 4 shows an implementation of the DAC bank using an $R-2R$ ladder network. Notice that the network has been modified slightly compared to the traditional architecture in that an extra switch has been introduced at the right-most $2R$ resistor to implement the one-bit DAC in Fig. 3(a). For the case of ideal circuit behavior, it is easy to verify that the node voltages V_j satisfy

$$V_j = V_j^{\text{ideal}} = \frac{V_{\text{REF}}}{2^{6-j}}. \tag{2}$$

It follows that the binary weighted currents I_j are given by

$$I_j = I_j^{\text{ideal}} = \frac{V_j}{2R}. \tag{3}$$

The output voltage $y_i[n]$ is dependent upon the currents flowing through the feedback resistor R_F such that

$$\begin{aligned} y_i[n] &= y_i^{\text{ideal}}[n] = R_F \sum_{j=0}^{5} I_j \\ &= \frac{R_F V_{\text{REF}}}{R 2^6} \left[x_i^{(0)}[n] + \sum_{j=1}^{5} 2^{j-1} x_i^{(j)}[n] \right]. \end{aligned} \tag{4}$$

With appropriate values of V_{REF}, R_F, and R, (4) can be made to equal (1) or a scaled version thereof, if desired. It will shortly be considered how nonideal circuit behavior affects the performance of the DAC bank.

The 8-bit version of the proposed DAC with randomization index 3 shown in Fig. 1 can easily be modified to accommodate other bit-resolutions and/or randomization indexes. For example, another layer of switching blocks, denoted layer 5, could be added. In this case, each of the switching blocks in this layer would have 5-bit outputs, and the number of DAC banks would increase two-fold to 16. The DAC banks would each consist of a 4-bit conventional DAC and a 1-bit conventional DAC. In general, more layers require more hardware, but—as will be shown—also provide greater suppression of harmonic distortion.

The switching blocks of the digital encoder can be constructed using binary switches [2]. The binary switch is a 2-input $\times$ 2-output device that simply either passes the inputs directly through to the outputs or connects the inputs to the outputs in reverse order, depending upon the value of $c_k[n]$. The hardware complexity of the digital encoder is a function of both the required number of binary switches and the required number of random control bits, and was discussed in detail in [2]. For convenience, the formulas dictating the hardware requirements of partial randomization DEM are repeated in the following. For a b-bit version of the DAC with randomization index I, the number of binary switches required is

$$N_{\text{bs}} = (b - I + 2)2^I - b - 2 \tag{5}$$

and the number of random control bits is simply

$$N_{\text{cb}} = I. \tag{6}$$

Thus, the 8-bit DAC of Fig. 1 requires 46 binary switches and three random control bits.

III. Performance Details

During each sample interval, the DAC-bank output $y_i[n]$ ideally equals the analog representation of its digital input $x_i[n]$. With this assumption, it was shown in [2] that interconnecting the switching blocks and DAC banks in the network of Fig. 1 results in a DAC for which

$$y[n] = x[n]. \tag{7}$$

However, in practice, the DAC banks operate such that

$$y_i[n] = x_i[n] + \Delta\{x_i[n]\} \tag{8}$$

where the $\Delta\{\cdot\}$ are errors associated with the 33 analog output levels that arise from nonideal circuit performance. As an example of how these errors might arise, consider again an implementation of the DAC bank using an $R-2R$ ladder network, as shown in Fig. 5. Nonideal IC fabrication

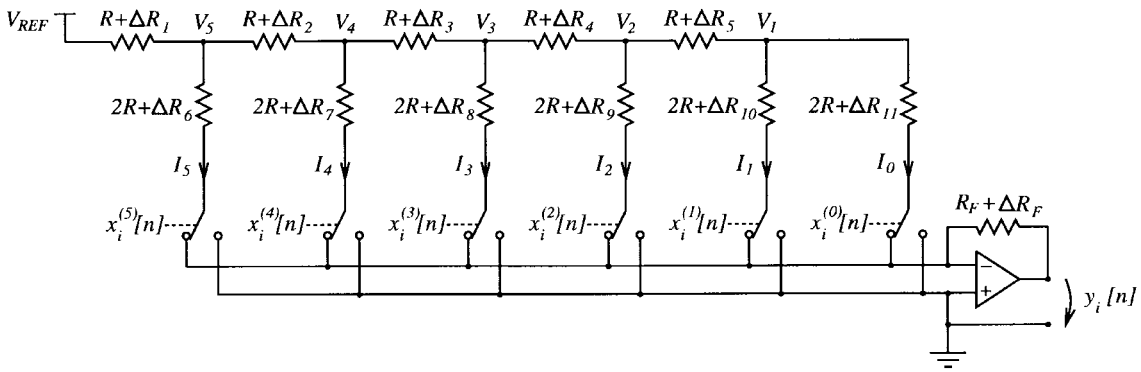


Fig. 5. The DAC bank implemented using an $R-2R$ ladder network with resistor errors and nonzero ohmic switch resistance.

processing and nonzero ohmic switch resistance result in errors, ΔR_k, of the resistor values and thus perturb the node voltages V_j. Specifically, the node voltages deviate from their ideal values given by (2) as

$$V_j = V_j^{\text{ideal}} + \Delta V_j \tag{9}$$

where the ΔV_j are functions of the resistor errors ΔR_k. As a consequence, the binary weighted currents into the op-amp summing node deviate by some quantity ΔI_j from their ideal values given by (3) according to

$$I_j = I_j^{\text{ideal}} + \Delta I_j. \tag{10}$$

It follows from (2) to (4), (9), and (10) that

$$\begin{aligned} y_i[n] &= (R_F + \Delta R_F)\left[\left(I_0^{\text{ideal}} + \Delta I_0\right)x_i^{(0)}[n] \right. \\ &\qquad \left. + \sum_{j=1}^{5}\left(I_j^{\text{ideal}} + \Delta I_j\right)x_i^{(j)}[n]\right] \\ &= y_i^{\text{ideal}}[n] + \sum_{j=0}^{5}\Delta_j\, x_i^{(j)}[n], \end{aligned}$$

where

$$\Delta_j = \Delta I_j R_F + \Delta R_F I_j. \tag{11}$$

Thus, each analog output level error can be written as a linear combination of the individual bits of $x_i[n]$.

The analog output level error of the DAC bank will subsequently be assumed to be of the form

$$\Delta\{x_i[n]\} = \sum_{j=0}^{5} e^{(j)}[n] \tag{12}$$

where

$$e^{(j)}[n] = \begin{cases} e_h^{(j)}, & \text{if } x_i^{(j)}[n] = 1; \\ e_l^{(j)}, & \text{if } x_i^{(j)}[n] = 0 \end{cases} \tag{13}$$

and where the $e_h^{(j)}$ and $e_l^{(j)}$ are time-invariant, but otherwise arbitrary, and are referred to as *static DAC-element errors*. Notice that (13) allows for asymmetric contributions of $x_i^{(j)}[n]$ in (12), depending upon whether $x_i^{(j)}[n]$ is zero or one. This form of the analog output level error accommodates for other popular architectures that can be used to realize the DAC bank, including the weighted resistor network DAC, the binary weighted current-steering DAC, and the charge scaling DAC [3].

With nonzero static DAC-element errors, it was shown in [2] that the DAC output has the form

$$y[n] = \alpha x[n] + \beta + e[n]$$

where α is a constant gain, β is a dc offset, and $e[n]$ is a conversion error term referred to as *DAC noise*.

A. Simulation Results

The performance of partial randomization DEM is demonstrated in Fig. 6 with simulation results of an example 8-bit version of the proposed DAC. The DAC banks were each simulated as an $R-2R$ ladder network with $R_F = 2R$. The resistor errors ΔR_k were chosen as samples of independent, normally distributed random variables with standard deviation $\sigma = 1\%$ relative to the nominal resistor values. Thus, the static DAC-element errors satisfied

$$e_h^{(j)} = \Delta_j \quad \text{and} \quad e_l^{(j)} = 0$$

with Δ_j given by (11). It should be emphasized that this particular choice of static DAC-element errors was made for simulation purposes only; the theoretical results developed in this paper do not depend upon any specific statistical distribution or correlation properties of the static DAC-element errors.

Each graph in Fig. 6 shows the simulated power spectral density (PSD) of $y[n]$ in decibels relative to $x_{\max}^2$, where $x_{\max} = 255$, when driving the DAC by a dithered and dc offset sinusoid. Specifically, $x[n]$ was formed by adding dither to the sequence $A\sin(\omega_0 n) + \text{DC}_x$, where $A = 126$, $\omega_0 = \frac{1275}{2048}\pi$, and $\text{DC}_x = 127.5$, and then quantizing the result to 8 bits. The dither added to the sinusoidal input was a white sequence with a triangular probability density function supported on $(-1, 1)$, so the quantization error was white noise [4].

Fig. 6(a) corresponds to an ideal DAC (i.e., a DAC with no static DAC-element errors, so $y[n] = x[n]$), and Fig. 6(b)–(d) corresponds to a DAC with nonzero static DAC-element errors and randomization indexes 1, 2, and 3, respectively.

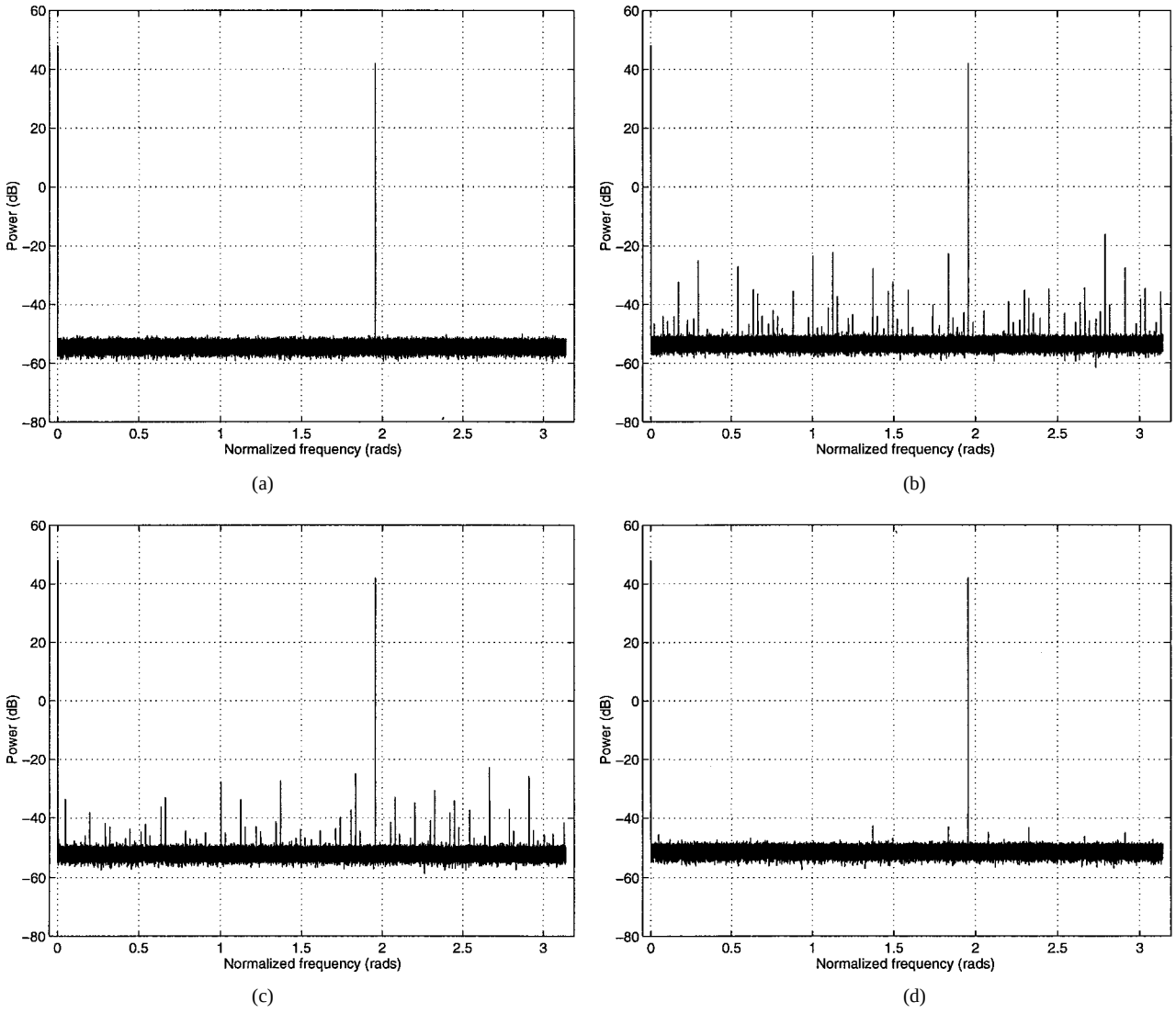


Fig. 6. Simulated PSD's relative to $x_{\max}^2$ of an example 8-bit DAC implemented using $R-2R$ ladder network DAC banks. The resistor errors were normally distributed of standard deviation $\sigma = 1\%$. Plot (a) shows the DAC input $x[n]$ (and thus the ideal DAC output $y[n]$), and (b)–(d) show the DAC output $y[n]$ with randomization indexes 1, 2, and 3, respectively.

As is evident from the numerous spurs distributed across the spectrum in Fig. 6(b), quite severe harmonic distortion results from the static DAC-element errors with only one layer of random switching. With the particular choice of static DAC-element errors used for the plots of Fig. 6, the maximum-amplitude spur occurs at a frequency of approximately 2.8π radians and has power 58.1 dB below the power of the desired sinusoidal signal. Thus, the SFDR provided by the DAC of this example is 58.1 dB. The simulation results of Fig. 6(c) and (d) indicate that the SFDR increases as the randomization index increases; the SFDR provided by the DAC in Fig. 6(c) is 64.7 dB, whereas the SFDR provided by the DAC in Fig. 6(d) is 84.6 dB. Additional simulations using other sinusoid frequencies yield similar findings.

Additional details of the simulation results are as follows. The PSD's were each estimated by averaging 16 length-2^{18} periodograms [5]. The frequency scales were normalized such that π corresponds to half the clock rate of the DAC.

B. Performance Equations

A complete theoretical analysis of partial randomization DEM is given in the appendixes. For the purpose of comparing simulation results and theory, this section presents the main results of the analysis.

Consider a b-bit version of the proposed DAC architecture with randomization index I, i.e., with random switching in layers $b-I+1, b-I+2, \cdots b$. Let $x[n]$ be a deterministic input sequence and let $x^{(j)}[n]$ denote the jth bit of $x[n]$, $1 \le j \le b$. In accordance with the usual definitions, let the *time-average means* of $x[n]$, $x^{(i)}[n]$, and $x^{(i)}[n]x^{(j)}[n]$ be defined as

$$\bar{M}_x = \lim_{P\to\infty} \frac{1}{P}\sum_{n=1}^{P} x[n], \quad \bar{M}_{x^{(i)}} = \lim_{P\to\infty} \frac{1}{P}\sum_{n=1}^{P} x^{(i)}[n],$$

and

$$\bar{M}_{x^{(i,j)}} = \lim_{P\to\infty} \frac{1}{P}\sum_{n=1}^{P} x^{(i)}[n]x^{(j)}[n],$$

respectively, and let the *time-average autocorrelation* of $x[n]$ be defined as

$$\bar{R}_{xx}[k] = \lim_{P\to\infty} \frac{1}{P}\sum_{n=1}^{P} x[n]x[n+k].$$

The time-average autocorrelation of $y[n]$ is defined analogously with x replaced by y in the above definition. The two main theoretical results of this paper can now be stated as follows.

Result 1: The DAC output can be written in the form

$$y[n] = \alpha x[n] + \beta + e[n] \tag{14}$$

where

$$e[n] = w[n] + s[n] \tag{15}$$

$w[n]$ is a zero-mean, white random process of the form

$$w[n] = \sum_{i=1}^{b} w_i[n]\, x^{(i)}[n] \tag{16}$$

$w_i[n]$ is a zero-mean, white sequence uncorrelated with $x[n]$, and $s[n]$ is a deterministic sequence of the form

$$s[n] = \sum_{i=1}^{b-I} s_i x^{(i)}[n]. \tag{17}$$

Appendix A provides formulas for the constants α and β in (14) and develops expressions for $w_i[n]$ in (16) and s_i in (17). For now, it suffices to know that the constant coefficients s_i depend only upon the static DAC-element errors.

Result 2: If $\bar{M}_x$ and $\bar{R}_{xx}[k]$ exist, then

$$\bar{R}_{yy}[k] = \bar{R}_{x_s x_s}[k] + \bar{\eta} + \bar{\sigma}^2\delta[k] \tag{18}$$

with probability 1, where

$$\bar{\eta} = 2\beta\bar{M}_{x_s} + \beta^2 \tag{19}$$

and

$$\bar{\sigma}^2 = \sum_{i=1}^{b}\gamma_i\bar{M}_{x^{(i)}} + \sum_{j=1}^{b-1}\sum_{i=j+1}^{b}\gamma_{i,j}\bar{M}_{x^{(i,j)}}. \tag{20}$$

In (18), $x_s[n]$ is the sequence resulting from lumping $\alpha x[n]$ and $s[n]$ together, i.e.,

$$x_s[n] = \alpha x[n] + s[n]. \tag{21}$$

Appendix B provides formulas for the constant coefficients γ_i and $\gamma_{i,j}$ in (20). For now, it suffices to know that these coefficients depend only upon the static DAC-element errors. It must be mentioned that Result 1 and Result 2 are independent of the underlying statistical distribution or any correlation properties of the static DAC-element errors.

C. Comparison of Simulation and Theory

To summarize, (14)–(17) imply that $y[n]$ consists of a scaled version of $x[n]$, a dc offset, and DAC noise $e[n]$, which consists of the sum of white noise $w[n]$ and a signal-dependent component $s[n]$. Thus, $s[n]$ accounts for *all* spurious tones present in $y[n]$, and, as can be seen from (17), the tones result from a linear combination of the input-bits $x^{(1)}[n]$ through $x^{(b-I)}[n]$. Given knowledge of $x[n]$ and the static DAC-element errors, these equations fully quantify all harmonic distortion present in $y[n]$.

The validity of the detailed knowledge of the spurious content of $y[n]$ implied by Result 1 can be demonstrated by computer simulation. As an example, each plot in Fig. 7 shows the simulated PSD relative to $x^2_{\max}$ of selected signals of the example 8-bit DAC used for Fig. 6(d). The DAC was driven by the same dithered and dc-offset sinusoid, and the randomization index was fixed at three. Fig. 7(a) shows the sequence $y[n] - x[n]$. As expected from (14), the resulting sequence appears to consist of a scaled version of $x[n]$, white noise, and spurious tones. Fig. 7(b) shows $e[n]$ formed as the sequence $y[n] - \alpha x[n] - \beta$, and it appears to consist of white noise and spurious tones. Fig. 7(c) shows $w[n]$ formed as the sequence $y[n] - \alpha x[n] - \beta - s[n]$, where $s[n]$ is given by (17). As expected, $w[n]$ appears to be a zero-mean, white noise random process. Fig. 7(d) shows the corresponding $s[n]$ as computed using (17). Notice that superimposing the results of Fig. 7(c) and (d) yields the results of Fig. 7(b), as expected from (15). Thus, the formulas for $y[n]$, $e[n]$, $w[n]$, and $s[n]$ are supported by the simulation results of Fig. 7.

The power of $w[n]$ is given by (20), and the validity of this expression can also be demonstrated using the simulation results of Fig. 7. Specifically, evaluating (20) for the simulated values of static DAC-element errors and the input sequence applied to the DAC yields a power of $w[n]$ of $\bar{\sigma}^2 = -54.14$ dB relative to $x^2_{\max}$. Numerically integrating the results of Fig. 7(c) yields -54.15 dB relative to $x^2_{\max}$, in agreement with the theoretical result.

D. An Interpretation of the Performance Equations

The theoretical results presented above are used in the following to develop a simple expression for the guaranteed minimum SFDR resulting from partial randomization DEM. A few definitions helpful in this development are first presented. Let $\mathcal{I}^+$ denote the set of indexes i in (17) such that $s_i > 0$, i.e.,

$$\mathcal{I}^+ = \{i : s_i > 0\} \tag{22}$$

and let $\mathcal{I}^-$ be the set of indexes i in (17) such that $s_i < 0$, i.e.,

$$\mathcal{I}^- = \{i : s_i < 0\}. \tag{23}$$

Let s^+ denote the sum of all positive s_i, i.e.,

$$s^+ = \sum_{i\in\mathcal{I}^+} s_i \tag{24}$$

let s^- denote the sum of all negative s_i, i.e.,

$$s^- = \sum_{i\in\mathcal{I}^-} s_i \tag{25}$$

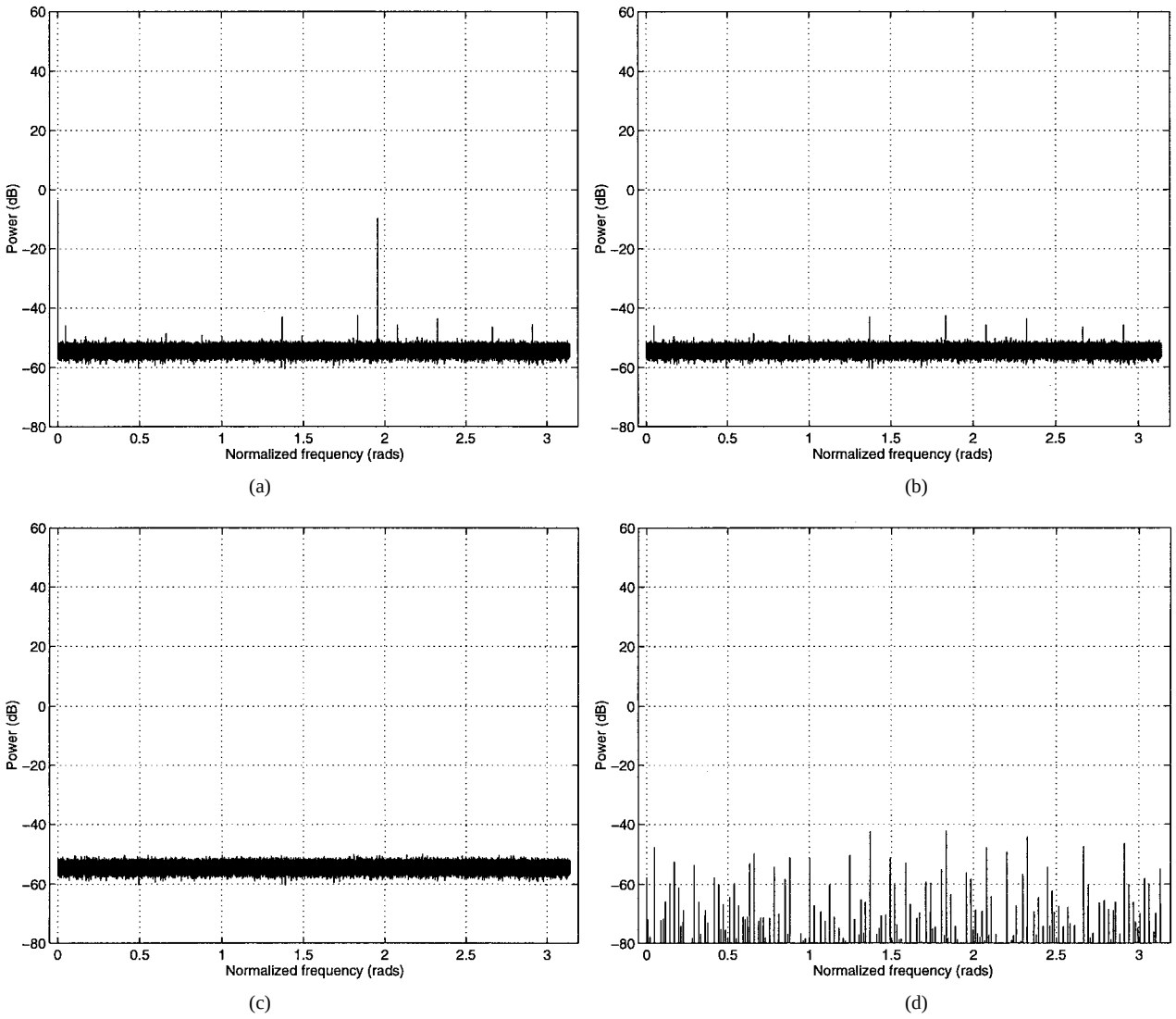


Fig. 7. Simulated PSD relative to $x_{\max}^2$ of selected signals of the example 8-bit DAC used for Fig. 6(d). The DAC was driven by the same dithered and dc-offset sinusoid, and the randomization index was fixed at three. (a) $y[n] - x[n]$. (b) $e[n]$. (c) $w[n]$. (d) $s[n]$.

and let $A_{s_{\max}}$ denote half the difference of s^+ and s^-, i.e.,

$$A_{s_{\max}} = \frac{(s^+ - s^-)}{2}. \tag{26}$$

Parseval's relation implies that the power of $s[n]$ equals the sum of the powers of the distinct spurs occurring in the PSD of $s[n]$. Thus, worst-case SFDR performance occurs when the power of $s[n]$ is at maximum and it consists of as few distinct spurs as possible. Since $s[n]$ is real, its PSD is symmetric, and the minimum number of distinct spurs is *two*, corresponding to nonzero frequencies ω_s and $-\omega_s$. Since $x^{(i)}[n] \in \{0, 1\}$, it follows from (17) that $s^- \leq s[n] \leq s^+$. Thus, worst-case total spur power is $A_{s_{\max}}^2$, and the power of each spur is bounded by $A_{s_{\max}}^2/2$. The amplitude of the signal component of $y[n]$ for a maximum-amplitude sinusoidal input signal is $\alpha x_{\max}/2$. It follows that the DAC provides an SFDR of at least $(\alpha x_{\max}/2A_{s_{\max}})^2$. Stating this result in debicels yields

$$\text{Minimum SFDR: } 20\log_{10}\left(\frac{\alpha x_{\max}}{2A_{s_{\max}}}\right) \text{ dB}. \tag{27}$$

IV. IC Fabrication Yield Estimation

With knowledge—or an assumption—of the statistical distribution of the static DAC-element errors, (20) allows for an IC fabrication yield estimation of the minimum SFDR provided by the DAC. The IC fabrication yield estimation procedure presented in the following was first introduced in [6] and is based upon the idea of computing a large number of samples of the parameter of interest for a given level of static DAC-element errors, thereby employing the law of large numbers to generate data that closely resemble the corresponding statistical distribution of the parameter.

An example IC fabrication yield estimation of the minimum SFDR computed using (27) and its supporting equations is shown in Fig. 8. Specifically, the figure shows the minimum SFDR for the 8-bit version of the DAC implemented using $R-2R$ ladder network DAC banks with normally distributed resistor errors of standard deviation σ ranging from 0.05% to 2%, and randomization index ranging from one to seven. Fig. 8(a)–(d) shows the smallest of the largest 5%, 35%, 65%, and 95% values, respectively. Each plot was based

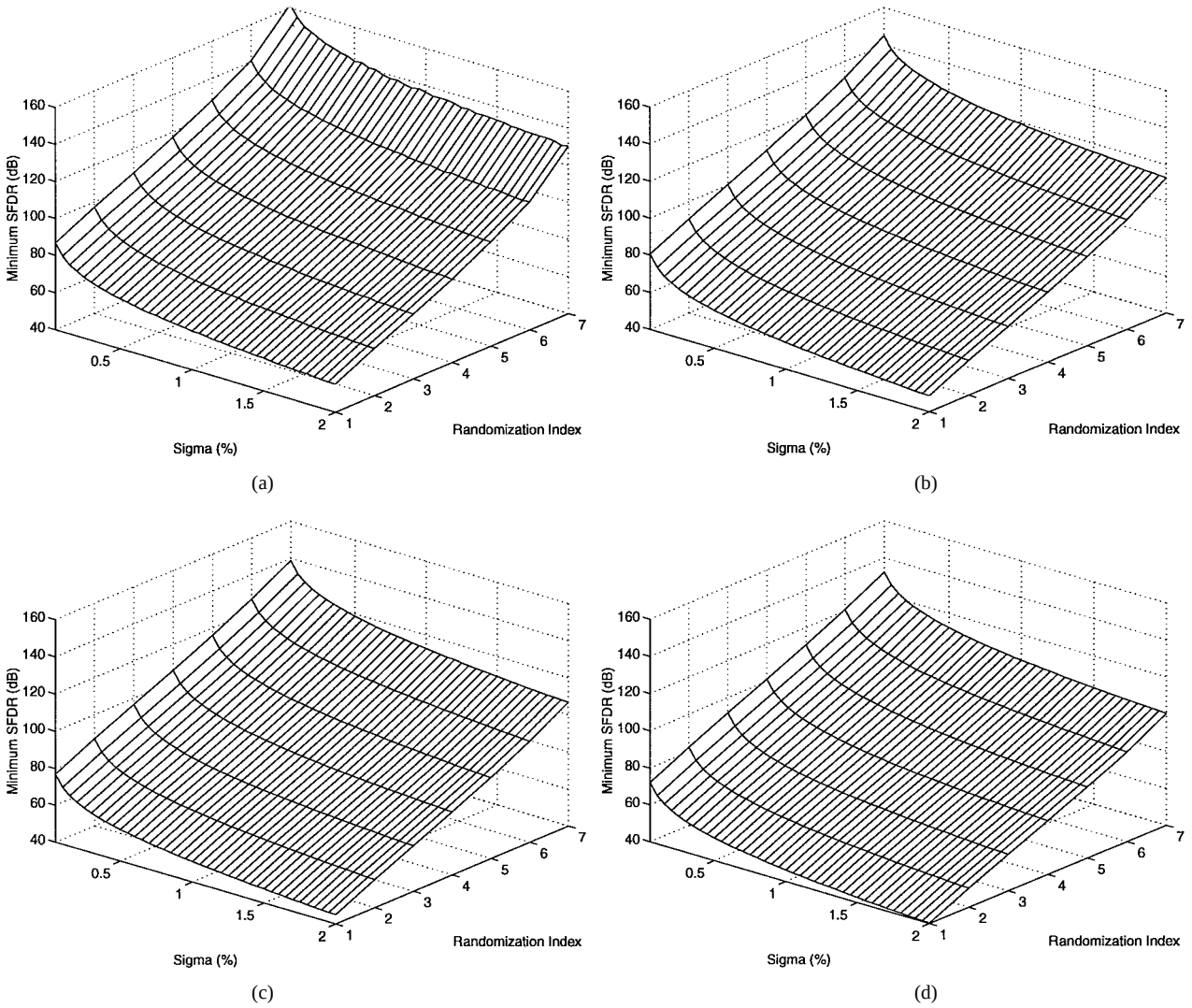


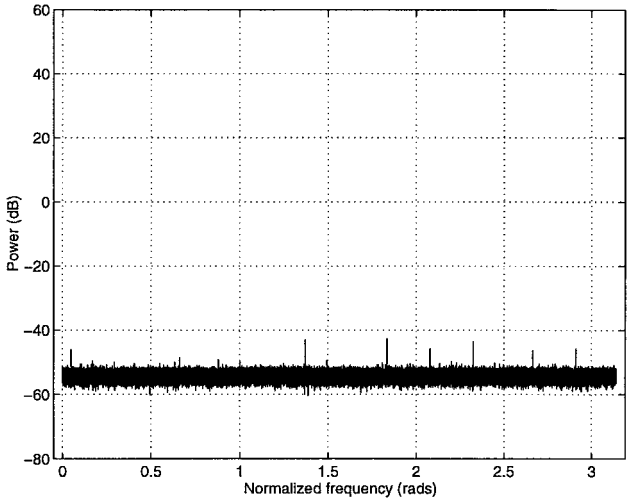
Fig. 8. An IC fabrication yield estimation of the minimum SFDR of the 8-bit version of the DAC implemented using $R-2R$ ladder network DAC banks. The resistor errors were normally distributed of standard deviation σ ranging from 0.05% to 2%, and the randomization index ranged from one to seven. The smallest of the largest (a) 5%, (b) 35%, (c) 65%, and (d) 95% values are plotted.

upon 10^4 calculated values. For example, with $\sigma = 1\%$ and randomization index three, Fig. 8(a) predicts that merely 5% of all 8-bit DAC's provide at least 81.0 dB SFDR, while Fig. 8(d) predicts that 95% of all 8-bit DAC's provide at least 65.7 dB SFDR. Thus, 90% of all 8-bit DAC's with randomization index three fabricated in a VLSI process resulting in normally distributed resistor errors with standard deviation $\sigma = 1\%$ satisfy

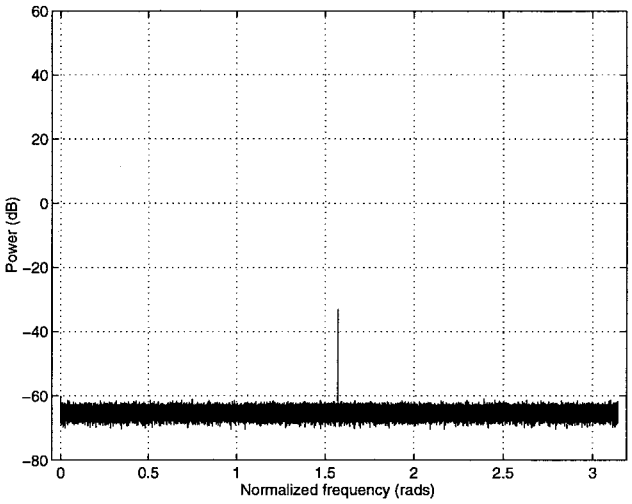
$$65.7 \text{ dB} \leq \text{Minimum SFDR} \leq 81.0 \text{ dB}. \tag{28}$$

An interesting conclusion to be drawn from Fig. 8 is that the estimated minimum SFDR increases by approximately 10 dB per unit increment of the randomization index, independent of the standard deviation of the resistor errors. Additional computations suggest that this conclusion generalizes to DAC's of any bit-resolution of interest. It should be mentioned that in the special case of full randomization DEM [2], i.e., with random switching in all eight layers, the DAC noise is fully uncorrelated with $x[n]$. Harmonic distortion is therefore completely eliminated and the DAC—in principle—provides an infinite SFDR. Thus, the 10-dB increase of the minimum SFDR per increment of the randomization index does not apply in the case of incrementing the number of random layers from seven to eight.

At first glance, the above estimates for the minimum SFDR achievable with partial randomization DEM may seem overly conservative given that the example 8-bit DAC used for the plots of Fig. 6 achieved an SFDR of 84.6 dB with randomization index three. Recall, however, that the IC fabrication yield estimation represents worst-case performance, where it is assumed that all power in $s[n]$ is lumped into *two* spurs occurring at frequencies $+\omega_s$ and $-\omega_s$. When driving the DAC by a (dithered) sinusoid, typically *many* spurs occur in the PSD of $e[n]$, as observed in Fig. 9(a), which is Fig. 6(b) repeated here for convenience. The occurrence of numerous spurs results in decreased power of the maximum-amplitude spur—and thus an increased SFDR—relative to worst-case performance. Fig. 9(b) shows the PSD of $e[n]$ of the same 8-bit DAC used for the plot of Fig. 9(a), but driven by a sequence $x[n]$ chosen such that the resulting PSD of $s[n]$ consists of



(a)



(b)

Fig. 9. Simulated PSD's of $e[n]$ relative to $x_{\max}^2$ of the example 8-bit DAC. The randomization index was fixed a three, and the plots show (a) $e[n]$ resulting from the dithered sinusoidal input, and (b) $e[n]$ resulting from an input sequence $x[n]$ chosen such that the PSD of $s[n]$ consists of only *two* spurs.

only two spurs. In this case, the maximum-amplitude spur has power −75.1 dB relative to $(\alpha x_{\max})^2/8$, in support of (28).

V. Conclusion

A detailed analysis of partial randomization DEM originally proposed in [2] has been presented. It was demonstrated using simulation results and shown with theory that harmonic distortion resulting from the static DAC-element errors is increasingly suppressed as the randomization index is increased. Specifically, it was observed that when implementing the DAC banks using $R-2R$ ladder networks with normally distributed resistor errors, the estimated minimum SFDR increases by approximately 10 dB per increment of the randomization index, independent of the particular DAC bit-resolution.

An IC fabrication yield estimation of the minimum SFDR has been presented that, given knowledge of the statistics of the static DAC-element errors, can be used in the design of a DAC with minimum hardware complexity while still providing the SFDR required for a given application.

Harmonic distortion resulting from inevitable nonideal circuit behavior such as clock-skew, nonlinear settling, and finite slew-rates has not been considered in this paper. Such nonideal circuit behavior is typically quite implementation-dependent, and research to quantify and mitigate its effects must likely be performed on a case-by-case basis. However, as has been shown, using partial randomization DEM, the harmonic distortion resulting from static DAC-element errors can be attenuated to the level of inevitable harmonic distortion, independent of the particular circuit technology.

Appendix A

The purpose of this appendix is to verify the form of the DAC output as stated by Result 1 of Section III.

1) Claim A: Consider a b-bit version of the proposed DAC architecture with randomization index I, $1 \le I < b$, i.e., with random switching in layers $b-I+1, b-I+2, \cdots, b$. In this case, the DAC banks consist of a $b-I$-bit conventional DAC and a 1-bit conventional DAC. Suppose that the analog output level error of the ith DAC bank is of the form given by the generalized versions of (12) and (13). Let $x[n]$ be a deterministic input sequence and let $x^{(j)}[n]$ denote the jth bit of $x[n]$, $1 \le j \le b$. The output of the DAC can then be written in the form

$$y[n] = \alpha x[n] + \beta + e[n] \tag{29}$$

where

$$e[n] = w[n] + s[n] \tag{30}$$

and $w[n]$ is a zero-mean, white random process of the form

$$w[n] = \sum_{i=1}^{b} w_i[n]\, x^{(i)}[n] \tag{31}$$

and $s[n]$ is a deterministic sequence of the form

$$s[n] = \sum_{i=1}^{b-I} s_i\, x^{(i)}[n]. \tag{32}$$

In (29)

$$\alpha = 1 + \frac{1}{2^b} \sum_{i=1}^{2^I} \sum_{j=0}^{b-I} \left(e_{h_i}^{(j)} - e_{l_i}^{(j)} \right) \tag{33}$$

and

$$\beta = \sum_{i=1}^{2^I} \sum_{j=0}^{b-I} e_{l_i}^{(j)}. \tag{34}$$

In (31), each $w_i[n]$ is a zero-mean, white random process of the form

$$w_i[n] = \begin{cases} w_{i,h_i}[n], & \text{if } i > b-I; \\ w_{i,h_i}[n] - s_i, & \text{if } i \le b-I; \end{cases} \tag{35}$$

where $w_{i,j}$ is shown in (36) at the bottom of the page and

$$h_i[n] = \begin{cases} \sum_{j=1}^{b-i} 2^j c_{i+j}[n] + (1 - c_i[n]) + 1, & \text{if } i > b - I \\ \sum_{j=1}^{I} 2^{j-1} c_{b-I+j}[n] + 1, & \text{if } i \le b - I. \end{cases} \tag{37}$$

In (32) and (35),

$$s_i = -\frac{1}{2^I} \sum_{k=1}^{2^I} \left(\sum_{\substack{j=1 \\ j \neq i}}^{b-I} w_{j,k} + e_{h_k}^{(0)} - e_{l_k}^{(0)} - (\alpha - 1) \right). \tag{38}$$

The above results do not depend upon any particular form or statistical properties of the static DAC-element errors.

Proof: To prove Claim A, several of the theoretical results developed in [2] will be used. For convenience, these are repeated in the following.

2) Results for Full Randomization DEM For a b-bit version of the DAC architecture with full randomization DEM, the output of the DAC can be written in the form

$$y[n] = \alpha x[n] + \beta + e[n] \tag{39}$$

where

$$\alpha = 1 + \frac{1}{2^b} \sum_{i=1}^{2^b} (e_{h_i} - e_{l_i}) \tag{40}$$

$$\beta = \sum_{i=1}^{2^b} e_{l_i} \tag{41}$$

and $e[n]$ is a zero-mean, white random process of the form

$$e[n] = \sum_{i=1}^{b} w_i[n] x^{(i)}[n]. \tag{42}$$

In (42), each $w_i[n]$ is a zero-mean, white random process of the form

$$w_i[n] = w_{i,h_i[n]} \tag{43}$$

where

$$w_{i,j} = \sum_{m=(j-1)2^{i-1}+1}^{j2^{i-1}} (e_{h_m} - e_{l_m}) - 2^{i-1}(\alpha - 1) \tag{44}$$

and

$$h_i[n] = \sum_{j=1}^{b-i} 2^j c_{i+j}[n] + (1 - c_i[n]) + 1. \tag{45}$$

The above results do not depend upon any particular form or statistical properties of the static DAC-element errors.

As explained in [2], partial randomization DEM with randomization index I is equivalent to full randomization DEM with the restriction that

$$c_k[n] = 1, \qquad \text{for } k = 1, 2, \cdots, b - I \tag{46}$$

so that the layers 1 through $b - I$ can be eliminated and substituted with an array of DAC banks, each consisting of a $b - I$-bit conventional DAC and a 1-bit conventional DAC. Specifically, since the static DAC-element errors of full randomization DEM are denoted e_{h_i} and e_{l_i}, $1 \le i \le 2^b$, the restriction (46) implies that the ith DAC bank operates according to (12) and (13), where the static DAC-element errors associated with the $b - I$-bit conventional DAC satisfy

$$e_{h_i}^{(j)} = \sum_{m=i2^{b-I}-2^{j-1}}^{i2^{b-I}-2^{j-1}} e_{h_m} \quad \text{and} \quad e_{l_i}^{(j)} = \sum_{m=i2^{b-I}-2^{j-1}}^{i2^{b-I}-2^{j-1}} e_{l_m} \tag{47}$$

and the static DAC-element errors associated with the 1-bit conventional DAC satisfy

$$e_{h_i}^{(0)} = e_{h_{i2^{b-I}}} \quad \text{and} \quad e_{l_i}^{(0)} = e_{l_{i2^{b-I}}}. \tag{48}$$

In the following, the results for partial randomization DEM stated in Claim A will be shown to be equivalent to the results for full randomization DEM with the restriction (46).

First, the formulas for α and β given by (33) and (34) are developed. As noted above, the results for full randomization DEM hold for *arbitrary* values of the static DAC-element errors e_{h_i} and e_{l_i}. In particular, if in (47)

$$e_{h_m} = e_{l_m} = 0 \quad \text{for } i2^{b-I} - 2^j + 1 \le m < i2^{b-I} - 2^{j-1} \tag{49}$$

then

$$e_{h_i}^{(j)} = e_{h_{i2^{b-I}-2^{j-1}}} \quad \text{and} \quad e_{l_i}^{(j)} = e_{l_{i2^{b-I}-2^{j-1}}}, \quad \text{for } j = 1, 2, \cdots, b - I. \tag{50}$$

It follows using (47)–(50) that for fixed value of i,

$$\sum_{j=(i-1)2^{b-I}+1}^{i2^{b-I}} (e_{h_j} - e_{l_j}) = \sum_{j=0}^{b-I} \left(e_{h_i}^{(j)} - e_{l_i}^{(j)} \right) \tag{51}$$

and thus

$$\sum_{i=1}^{2^b} (e_{h_i} - e_{l_i}) = \sum_{i=1}^{2^I} \sum_{j=0}^{b-I} \left(e_{h_i}^{(j)} - e_{l_i}^{(j)} \right)$$

$$w_{i,j} = \begin{cases} \sum_{m=(j-1)2^{i-b+I-1}+1}^{j2^{i-b+I-1}} \sum_{k=0}^{b-I} \left(e_{h_m}^{(k)} - e_{l_m}^{(k)} \right) - 2^{i-1}(\alpha - 1), & \text{if } i > b - I \\ e_{h_j}^{(i)} - e_{l_j}^{(i)} - 2^{i-1}(\alpha - 1), & \text{if } i \le b - I \end{cases} \tag{36}$$

which shows that (33) is equivalent to (40). Similarly,

$$\sum_{i=1}^{2^b} e_{l_i} = \sum_{i=1}^{2^I} \sum_{j=0}^{b-I} e_{l_i}^{(j)}$$

which shows that (34) is equivalent to (41).

Next, (35)–(38) detailing the form of the DAC noise will be verified. For the case $i > b - I$, it is straightforward to show that (35)–(37) follow from (42)–(45). Specifically, it suffices to show that (36) is equivalent to (44). For this purpose, the use of (51) and some algebraic manipulations result in

$$\sum_{k=(j-1)2^{i-1}+1}^{j2^{i-1}} (e_{h_k} - e_{l_k}) = \sum_{m=(j-1)2^{i-b+I-1}+1}^{j2^{i-b+I-1}} \sum_{k=0}^{b-I} \left(e_{h_m}^{(k)} - e_{l_m}^{(k)} \right)$$

which suffices to show the asserted result. Notice that it follows directly from [2] that $w_i[n]$ is zero-mean, since the possible values of $w_i[n]$ are unaffected by (46).

For the case $i \leq b - I$, it will first be shown that $w_{i,j}$ in (36) with subscript defined by (37) is equivalent to $w_{i,j}$ in (44) with subscript defined by (45) and the restriction (46). For this purpose, notice that with the restriction (46), it follows after some algebraic manipulations that (45) can be written as

$$h_i[n] = \left(\sum_{j=1}^{I} 2^{j-1} c_{b-I+j}[n] + 1 \right) 2^{b-I+1-i} - 1. \quad (52)$$

Thus, if in (37) $h_i[n] = j$, it follows that (52) may be written as

$$h_i[n] = j2^{b-I+1-i} - 1.$$

But, as follows from (44) and some algebraic manipulations

$$w_{i,j2^{b-I+1-i}-1} = \sum_{m=j2^{b-I}-2^i+1}^{j2^{b-I}-2^{i-1}} (e_{h_m} - e_{l_m}) - 2^{i-1}(\alpha - 1)$$

which—referring to (47)—is equivalent to (36), as asserted. It will next be shown that $w_i[n]$ is zero-mean. It follows from (43)–(45) that the effect of the restriction (46) is to reduce the set of possible values of $w_i[n]$ to a subset of the set of values otherwise possible. Therefore, with the restriction (46), $w_i[n]$ in (43) is a white random process, generally with a nonzero mean value. Denoting this mean value s_i, (42) may be written as

$$e[n] = \sum_{i=b-I+1}^{b} w_i[n]\, x^{(i)}[n] + \sum_{i=1}^{b-I} (w_i[n] - s_i)\, x^{(i)}[n] + \sum_{i=1}^{b-I} s_i\, x^{(i)}[n].$$

Defining the white, *zero-mean* random processes $w_i[n]$ as in (35) results in

$$e[n] = \sum_{i=1}^{b} w_i[n]\, x^{(i)}[n] + \sum_{i=1}^{b-I} s_i x^{(i)}[n]$$

or, referring to (31) and (32)

$$e[n] = w[n] + s[n]$$

as asserted in (30). It remains to verify (38) by establishing that $w_i[n]$ in (35) is indeed zero-mean. From (37) it follows that there are 2^I possible equally probable values of $w_i[n]$. Specifically, during the nth sample period

$$w_i[n] = w_{i,j} - s_i, \quad \text{where } j \in \{1, 2, \cdots, 2^I\}.$$

Then, by definition

$$E\{w_i[n]\} = \frac{1}{2^I} \sum_{j=1}^{2^I} (w_{i,j} - s_i)$$

and defining s_i as in (38) yields

$$\begin{aligned} E\{w_i[n]\} &= \frac{1}{2^I} \sum_{j=1}^{2^I} \left(\sum_{i=1}^{b-I} w_{i,j} + e_{h_j}^{(0)} - e_{l_j}^{(0)} - (\alpha - 1) \right) \\ &= \frac{1}{2^I} \sum_{j=1}^{2^I} \left(\sum_{i=0}^{b-I} (e_{h_j}^{(i)} - e_{l_j}^{(i)}) - 2^{b-I}(\alpha - 1) \right) \\ &= \frac{1}{2^I} (2^b(\alpha - 1) - 2^b(\alpha - 1)) \\ &= 0 \end{aligned}$$

as asserted. □

APPENDIX B

This appendix states and proves an expression for the variance of the zero-mean, white random process $w[n]$.

1) Claim B: The variance of $w[n]$ is given by

$$\mathrm{Var}\{w[n]\} = \sum_{i=1}^{b} \gamma_i\, x^{(i)}[n] + \sum_{j=1}^{b-1} \sum_{i=j+1}^{b} \gamma_{i,j}\, x^{(i)}[n] x^{(j)}[n]$$

where

$$\gamma_i = \begin{cases} \dfrac{1}{2^{b-i+1}} \displaystyle\sum_{j=1}^{2^{b-i+1}} (w_{i,j})^2, & \text{if } i > b - I \\ \dfrac{1}{2^I} \displaystyle\sum_{j=1}^{2^I} (w_{i,j} - s_i)^2, & \text{if } i \leq b - I; \end{cases} \quad (53)$$

and $\gamma_{i,j}$ is shown in (54) at the top of the next page.

Proof: Since $w[n]$ is zero-mean, $\mathrm{var}\{w[n]\} = E\{(w[n])^2\}$, where $E\{\cdot\}$ denotes the statistical expectation operator. Using (16) and rearranging terms results in

$$\mathrm{Var}\{w[n]\} = \sum_{i=1}^{b} E\{(w_i[n])^2\} x^{(i)}[n] + 2 \sum_{j=1}^{b-1} \sum_{i=j+1}^{b} E\{w_i[n] w_j[n]\} x^{(i)}[n] x^{(j)}[n]. \quad (55)$$

Consider first $E\{(w_i[n])^2\}$. As indicated by (35), two cases are of interest.

For $i > b - I$, the corresponding result in Appendix B of [2] is directly applicable to obtain the result asserted in (53), since the possible values of $w_i[n]$ are unaffected by (46).

For $i \leq b - I$, it follows from (37) that there are 2^I possible equally probable values of $w_i[n]$, dictated by $c_k[n], k = b-I+1, b-I+2, \cdots, b$. Using (35) and applying the definition of statistical expectation gives the result asserted in (53).

Consider next $E\{w_i[n] w_j[n]\}$, where $1 \leq j < i \leq b$. Three cases are of interest.

$$\gamma_{i,j} = \begin{cases} \dfrac{1}{2^{b-j-1}} \displaystyle\sum_{k=1}^{2^{b-i}} w_{i,2k-1} w_{i,2k}, & \text{if } i,j > b-I; \\ \dfrac{1}{2^{I-1}} \displaystyle\sum_{l=0}^{1} \sum_{k=0}^{2^{b-i}-1} w_{i,2(k+1)-l} \sum_{m=0}^{2^{i-b+I-1}-1} \left(w_{j,2^{i-b+I-1}(2k+l)+m} - s_j\right), & \text{if } i > b-I, j \le b-I; \\ \dfrac{1}{2^{I-1}} \displaystyle\sum_{k=1}^{2^I} (w_{i,k} - s_i)(w_{j,k} - s_j), & \text{if } i,j \le b-I. \end{cases} \tag{54}$$

For $i,j > b-I$, the corresponding result in Appendix B of [2] is directly applicable to obtain the result asserted in (53).

For $i,j \le b-I$, the probability of a specific value of $w_i[n]$ is $\frac{1}{2^I}$, as discussed above. It follows from (37) that the value of $w_j[n]$ fully depends upon $w_i[n]$; suppose that the value of $w_i[n]$ is $w_{i,k} - s_i$ for some $k \in \{1,2,\cdots,2^I\}$. Then there is only *one* possible value of $w_j[n]$, namely $w_{j,k} - s_j$. Applying the definition of statistical expectation—and accounting for the factor of two occurring in (55)—gives the result asserted in (54).

For $i > b-I$ and $j \le b-I$, each of the 2^{b-i+1} possible values of $w_i[n]$ occurs with probability $1/2^{b-i+1}$. From (37) it follows that for integer parameters k and l

$$w_i[n] = w_{i,2(k+1)-l}, \quad \text{where}$$
$$k \in \{0,1,\cdots,2^{b-i}-1\} \quad \text{and} \quad l \in \{0,1\}. \tag{56}$$

For fixed value of $w_i[n]$, i.e., for fixed values of k and l in (56), there are $2^{i-b+I-1}$ possible equally probable values of $w_j[n]$. Using (37) and a number of algebraic manipulations, these values can be expressed in terms of k, l, and an integer parameter m as

$$w_j[n] = w_{j,2^{i-b+I-1}(2k+l)+m} - s_j, \quad \text{where}$$
$$m \in \{0,1,\cdots,2^{i-b+I-1}-1\}.$$

Again, applying the definition of statistical expectation—and accounting for the factor of two occurring in (55)—verifies the result asserted in (54). □

APPENDIX C

The purpose of this appendix is to verify the time-average properties of the DAC output as stated in Result 2 of Section III.

1) Claim C: If $\bar{M}_x$ and $\bar{R}_{xx}[k]$ exist, then $\bar{R}_{yy}[k]$ is given by (19), (20), and (21) with probability one. In (20), γ_i and $\gamma_{i,j}$ are given by (53) and (54), respectively.

Proof: From Claim A and (21) it follows that

$$y[n] = x_s[n] + \beta + w[n].$$

The statistical autocorrelation of $y[n]$ can then be written in the form

$$R_{yy}[n,k] = E\{(x_s[n] + \beta + w[n])(x_s[n+k] + \beta + w[n+k])\}.$$

It is easy to verify that if $\bar{M}_x$ and $\bar{R}_{xx}[k]$ exist, then $\bar{M}_{x_s}$ and $\bar{R}_{x_s x_s}[k]$ exist, since α and the s_i are finite. Arguments fully identical to those presented for the corresponding result in [2] can then be used to establish Claim C. □

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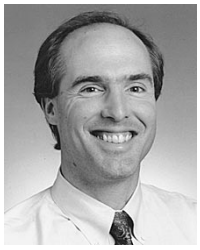

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