A Nyquist-Rate Delta–Sigma A/D Converter

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***Abstract*— This paper describes an analog-to-digital converter which combines multiple delta–sigma modulators in parallel so that time oversampling may be reduced or even eliminated. By doubling the number of Lth-order delta–sigma modulators, the resolution of this architecture is increased by approximately L bits. Thus, the resolution obtained by combining M delta–sigma modulators in parallel with no oversampling is similar to operating the same modulator with an oversampling rate of M. A parallel delta–sigma A/D converter implementation composed of two, four, and eight second-order delta–sigma modulators is described that does not require oversampling. Using this prototype, the design issues of the parallel delta–sigma A/D converter are explored and the theoretical performance with no oversampling and with low oversampling is verified. This architecture shows promise for obtaining high speed and resolution conversion since it retains much of the insensitivity to nonideal circuit behavior characteristic of the individual delta–sigma modulators.**

***Index Terms*— Converters, integrated circuit design, parallel architectures.**

I. Introduction

ANALOG-TO-DIGITAL converters are key components in many modern electronic systems. They provide the critical translation of a measured analog signal to a digital representation. Once in digital form, the data can be easily and accurately processed to extract the information desired. The process of converting the analog signal to a digital signal often limits the speed and resolution of the overall system. As a result, there is a need to develop A/D converters that achieve both high speed and resolution. In particular, many imaging, communication, and instrumentation systems may benefit from such converters.

The Flash A/D converter provides the highest conversion rate of all the A/D architectures for a given technology. This architecture uses $2^n - 1$ 1-b A/D converters (i.e., comparators) operating in parallel followed by digital decoding logic to convert an analog signal into a digital signal with n bits of resolution. While the parallelism allows for very high-speed conversion, the accuracy of the converted signal is limited by the analog component matching within the converter. Additionally, the area increases exponentially as the number of bits increases. Thus, typically no more than 10 b of resolution are obtained without component trimming and excessive area consumption using a Flash A/D converter.

In contrast, the delta–sigma $(\Delta\Sigma)$ A/D converter is not limited by the component matching. It uses time oversampling to increase the resolution in amplitude [1] and resolutions as high as 20 b have been demonstrated with this architecture [2]. Unlike other A/D converter architectures, this architecture does not rely on high precision analog components, and the resolution of an Lth-order delta–sigma A/D converter is increased by $L + 1/2$ bits for each doubling in the oversampling ratio. Unfortunately, the need for high oversampling in $\Delta\Sigma$ A/D converters has limited their use to primarily low-frequency applications. Thus, it would seem advantageous to combine $\Delta\Sigma$ A/D converters in parallel to extend the bandwidth of these converters while maintaining the high resolution. Using such an approach, the conversion rate of the overall delta–sigma A/D converter can, in theory, be increased without loss in resolution.

One approach of combining multiple $\Delta\Sigma$ A/D converters in parallel consists of simultaneously applying the input to M delta–sigma modulators. The outputs of the $\Delta\Sigma$ modulators are digitally combined and then filtered. Assuming sufficient circuit noise, the signal power adds in amplitude $(x_1 + x_2 + \cdots x_M)^2$ while the quantization error will be uncorrelated and thus adds in power $(e_1^2 + e_2^2 + \cdots e_M^2)$. As a result, the signal-to-noise ratio (SNR) increases by 3 dB for each doubling in the number of channels. Because doubling the hardware results in only a 1/2-b increase in the resolution, this parallel approach is extremely area inefficient.

The parallel delta–sigma $(\Pi\Delta\Sigma)$ A/D architecture described here combines multiple delta–sigma modulators in parallel along with analog preprocessing of the input signal and digital postprocessing of the output signals to achieve an increase of L bits for each doubling in the number of Lth-order delta–sigma modulators [3]. This is nearly the same gain obtained from doubling the oversampling ratio in a single Lth-order modulator. The $\Pi\Delta\Sigma$ A/D converter maintains much of the insensitivity to component matching characteristic of the conventional delta–sigma modulator. An added feature of the $\Pi\Delta\Sigma$ A/D converter is that oversampling is not required.

In this paper, the parallel delta–sigma architecture is briefly described in Section II. Section III presents the performance obtained with the $\Pi\Delta\Sigma$ A/D converter. The circuit design considerations of a second-order $\Delta\Sigma$ modulator used in this parallel architecture are analyzed in Section IV. Section V describes the design implementation and the experimental results that verify the operation of this parallel architecture at both the full-rate (Nyquist rate) and with moderate oversampling. The

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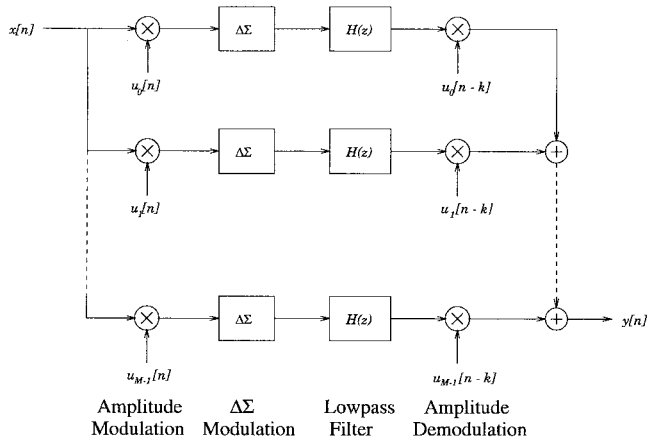

Fig. 1. The $\Pi\Delta\Sigma$ A/D architecture with analog input $x[n]$ and digital output $y[n]$.

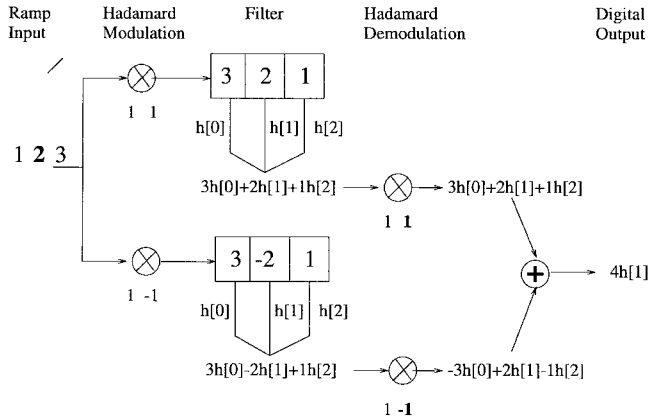

Fig. 2. Illustration of the $\Pi\Delta\Sigma$ A/D converter operation. A ramp signal is applied to the input of each channel, scaled by the center tap of the filter, and summed at the output of the filters. Notice that the output corresponding to an input of 2 is twice as large since the signal on each channel adds. The Hadamard modulation makes it so that the signal sees only the center tap of the filter (in this case h[1]), therefore it is all-pass filtered. The quantization noise in not passed through the Hadamard modulator, and thus it sees all taps of the filter.

measurements provide further insight into the design so that future implementations can potentially exceed the performance of existing A/D converters.

II. The Parallel $\Delta\Sigma$ A/D Converter Architecture

The $\Pi\Delta\Sigma$ A/D converter architecture is shown in Fig. 1 [3], [4]. The analog input $x[n]$ is simultaneously applied to M amplitude modulators each followed by a conventional delta–sigma modulator. The $\Delta\Sigma$ modulator outputs are then filtered, demodulated, and summed together to produce a single digital output sequence. In the conventional $\Delta\Sigma$ A/D converter, both the signal and the quantization noise pass through the same filter, and therefore, both are filtered by the same low-pass decimation filter. In contrast, the $\Pi\Delta\Sigma$ A/D converter *amplitude modulates* the input to decouple the signal from the quantization noise such that the filtering of the signal is undone by *amplitude demodulation*. In effect, the signal is simply delayed while the noise is low-pass filtered. Thus, the cutoff frequency of the quantization noise filter may be lower than the signal bandwidth, which makes A/D conversion without oversampling possible.

The amplitude modulators used in this architecture can be derived from any unitary matrix. Hadamard modulation has been chosen since it consists of plus and minus ones, and therefore it is easy to realize in an actual implementation. Additionally, Hadamard modulators maximize the signal-to-noise ratio of the A/D converter because the signal on each channel adds coherently at the output. The Hadamard matrix is defined as

$$H_i = \begin{bmatrix} H_{i-1} & H_{i-1} \\ H_{i-1} & -H_{i-1} \end{bmatrix} \quad \text{where} \quad H_0 = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}. \tag{1}$$

As an example, the modulation sequence for a four-channel converter is

$$H = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix}.$$

Each row represents the modulation sequence for one channel of the $\Pi\Delta\Sigma$ A/D converter. Notice that even for the four-channel case, the signals on each channel are not simply frequency decomposed. Channels 3 and 4 actually are modulated at the same frequency but differ by the phase component.

To illustrate the operation of the parallel architecture, a two-channel example is provided in Fig. 2. To show the effect of the system on the signal, it is assumed that the signal is only delayed by the delta–sigma modulators. A ramp signal is applied at the input of each channel and multiplied by the appropriate Hadamard sequence: all one's on the first channel and alternating one and minus one on the second channel. The output is stored in the registers of the filter as shown in the figure. These values are then multiplied by the corresponding filter coefficients, summed together, and demodulated by a time-shifted version of the Hadamard sequence (one on the first channel and minus one on the second channel). When the outputs of the digital filters are summed, notice that the input signal (2 in this example) is only multiplied by the center tap of the filter and it is two times larger (corresponding to the number of channels). In effect, the input signal passes to the output of each channel without being filtered. Because the signal sees only the center tap of the filter, the other filter coefficients may be chosen to optimally suppress the quantization noise.

The time-interleaved A/D converter is similar to the $\Pi\Delta\Sigma$ A/D converter [5]. Instead of a Hadamard sequence multiplying the input and output, an identity matrix is used. With the identity matrix, the signal magnitude is decreased by a factor of M (where M is the number of channels) over the Hadamard modulation because the signal passes through only one channel at any given time. Thus, the $\Pi\Delta\Sigma$ A/D converter provides 1/2 b more improvement in SNR when the number of channels are doubled.

III. Performance of the $\Pi\Delta\Sigma$ A/D Converter

The quantization noise from each channel of the $\Pi\Delta\Sigma$ A/D converter adds in power at the output. Assuming the variance

of the quantization error is $\Delta^2/12$, where Δ is the quantization step-size, the time-average power of the quantization error is

$$P_e = \frac{1}{2\pi}\,\frac{M\Delta^2}{12}\,\int_{-\pi}^{\pi} |N(e^{j\omega})H(e^{j\omega})|^2\,d\omega \qquad (2)$$

where M is the number of channels, $N(z)$ is the $\Delta\Sigma$ modulator quantization noise filter, and $H(z)$ is the digital filter impulse response (which is the same for each channel). If the signal is simply delayed by the $\Delta\Sigma$ modulator, i.e., the signal transfer function is $S(z) = z^{-m}$ where m is the signal delay, an optimal form for $H(z)$ which minimizes P_e for a given filter length can be determined [3]. It is an odd N-tap FIR filter with the following constraints:

$$h(n) = \begin{cases} 0 & \text{for } n < 0; \\ \dfrac{1}{M} & \text{for } n = \dfrac{N-1}{2} \\ 0 & \text{for } n = \dfrac{N-1}{2} + iM, \quad i = \pm 1, \pm 2, \cdots \\ 0 & \text{for } n \le N. \end{cases} \qquad (3)$$

Notice that only certain values of $h(n)$ are constrained. The remainder can be chosen so as to minimize the amount of quantization noise at the output. The length of the filter will affect the sharpness of the passband-to-stopband transition but will not affect the cutoff frequency. Simulation has shown that no significant reduction in the quantization noise results for filter lengths greater than $2LM$ where L is the order of the modulator and M is the number of channels in the $\Pi\Delta\Sigma$ A/D converter. Some realizations of this A/D converter may give prohibitively large filters due to the noninteger coefficients within the digital filter. An efficient alternative is to use comb^{L+1} filters [3]. They attenuate the quantization noise to nearly the same extent as the optimal filters [9].

The magnitude response of the optimal filters for two, four, eight, and 16 channels is plotted in Fig. 3. In each case, the -3 dB frequency is marked. Note that while all of these $\Pi\Delta\Sigma$ A/D filters enable conversion up to the Nyquist frequency, the actual filter cutoff is halved as the number of channels is doubled. Thus, less quantization noise is included as the number of channels is increased. This is analogous to the conventional $\Delta\Sigma$ A/D converter where as the oversampling ratio is increased, less quantization noise is included. Again, this property is only possible because the filtering of the signal is *undone* by the Hadamard demodulation.

The resolution in bits of the $\Pi\Delta\Sigma$ A/D converter without oversampling is given by

$$B = \frac{1}{2}\,\log_2\left[\frac{4}{P_e}\right] \qquad (4)$$

where the useful range of the converter is assumed to be the entire output range of the feedback DAC. Fig. 4 shows the ideal $\Pi\Delta\Sigma$ A/D converter performance with second-, third- and fourth-order $\Delta\Sigma$ modulators and with filters of sufficient length such that no appreciable gain in performance is obtained by further increasing the filter length. The increase in resolution is approximately L bits for each doubling of the number of channels. Recall that the increase in resolution is

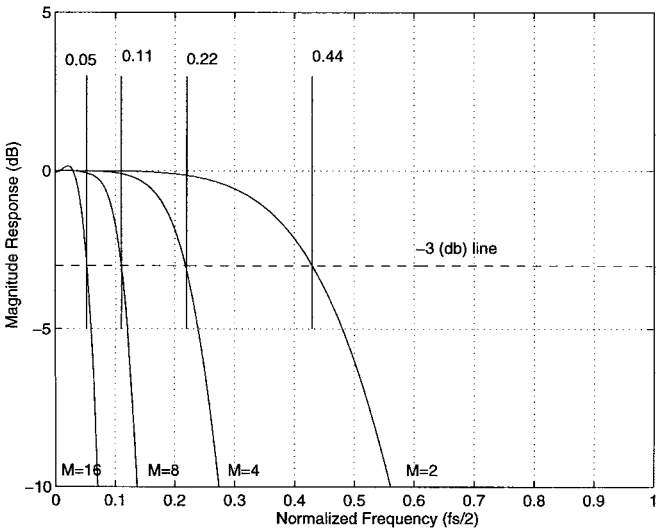

Fig. 3. Example of the magnitude response of the optimal filters in the $\Pi\Delta\Sigma$ A/D converter with two, four, eight, and 16 channels. The -3 dB frequency is shown by the marker for each case.

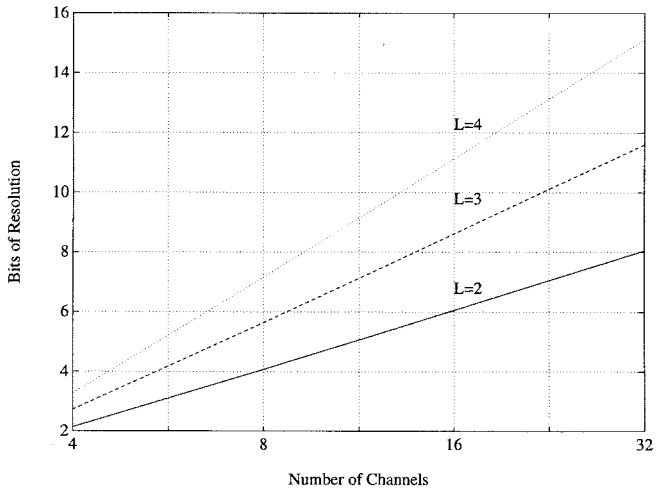

Fig. 4. The resolution of the $\Pi\Delta\Sigma$ A/D converter (with an input at -6 dB) versus the number of channels, M as predicted by theory. The dynamic range is approximately 1 b higher than shown.

$L + \frac{1}{2}$ bits for each doubling in the oversampling ratio for a single-channel oversampled Lth-order $\Delta\Sigma$ A/D converter. The increase in resolution as the number of channels is doubled is L bits since the quantization noise is doubled over a single-channel case.

The parallelism in the $\Pi\Delta\Sigma$ A/D converter can also be combined with oversampling. In this case, each column of the Hadamard sequence is repeated by the number of times corresponding to the oversampling ratio. As with the full-rate converter, a comb filter may be used as an efficient filter. Additionally, an equalization filter must follow this filter to compensate for the signal filtering [8].

IV. Design Considerations

A. Channel Matching

Several sources of errors in the $\Pi\Delta\Sigma$ A/D converter including Hadamard modulation gain errors and offsets, offsets at the

TABLE I
RELATIVE SENSITIVITY TO CHANNEL MATCHING OF THE $\Pi\Delta\Sigma$ A/D CONVERTER WHERE 0 = MODERATELY SENSITIVE, $-$ = INSENSITIVE, AND $+$ = VERY SENSITIVE

Channel Error	Sensitivity	Comments
Offset before Hadamard Mod.	-	DC offset of input signal
Hadamard gain errors	0	Harmonic distortion and tones generated
Hadamard offsets	0	Harmonic distortion and tones generated
Offset at input of $\Delta\Sigma$ Mod.	++	Generates tones, can be cancelled
Integrator gain errors	-	Very insensitive
DAC gain errors	-	Linearity must be M times better than system requirement
DAC offset	++	Same as offset at input, Generates tones, can be cancelled

input of the $\Delta\Sigma$ modulators, integrator gain errors, and DAC gain errors and offsets were evaluated. Table I summarizes the relative sensitivity of the parallel delta–sigma A/D converter to each of these errors.

The $\Pi\Delta\Sigma$ A/D converter is most sensitive to offsets at the input of the individual $\Delta\Sigma$ modulators and offsets in the DAC. Since the $\Pi\Delta\Sigma$ filters are low pass, the offset of each channel is passed by its $\Delta\Sigma$ modulator, and it is therefore retained at the output of its respective filter. When the filter outputs are demodulated, these offsets are spread throughout the spectrum and appear at the final output as illustrated in Fig. 5. Fig. 5(a) is the $\Delta\Sigma$ modulator output on the first channel of an 16-channel $\Pi\Delta\Sigma$ A/D converter. The dc offset is indicated by the arrow. Fig. 5(b) shows the overall output. Because of the Hadamard demodulation, the offset introduces tones throughout the frequency spectrum at multiples of 1/16th (or one over the number of channels) of the clock frequency. The errors due to the dc offset, although spread throughout the frequency spectrum, are signal independent. The mean squared error due to the offset is simply the square of the sum of the offsets on the individual channels

$$\text{mse} = \sum_{j=1}^{M-1} f_j^2 \tag{5}$$

where f_j is the offset on the jth channel and M is the total number of channels. The offset of the first channel appears as the offset of the overall A/D converter so it may be ignored in this analysis. Assuming σ_f is the standard deviation of the channel offset, then the total expected error due to the channel offset is $(M-1)\sigma_f^2$. As the number of channels increases, the mean squared error also increases for the same channel offset. Thus, to obtain N bits of resolution, the variance of the channel offset must be $M-1$ times lower than this noise floor requirement. Although the $\Pi\Delta\Sigma$ converter is sensitive to channel offset, it can be easily measured at the output of the modulator and then digitally cancelled.

The $\Pi\Delta\Sigma$ A/D converter is insensitive to channel mismatches due to integrator gain errors particularly for second-order modulators. This is obvious when we examine the signal path in the $\Pi\Delta\Sigma$. In the second-order delta–sigma modulator, the gain of the second integrator is absorbed by the quantizer gain. As a result, the insensitivity to the second integrator gain in a single channel is preserved when it is placed in the parallel structure. The $\Pi\Delta\Sigma$ A/D converter is also insensitive to the gain of the first integrator in the delta–sigma modulator. But like the $\Delta\Sigma$ A/D converter, it is sensitive to DAC gain errors. However, if a single-bit quantizer is used and the same capacitor is used for input sampling and implementation of the DAC, the sensitivity to the DAC gain is reduced. Using the same capacitor requires scaling the analog input to avoid overloading the quantizer. Hadamard gain errors and offset errors introduce harmonic distortion and generate tones but at levels much lower than the DAC gain errors and offsets.

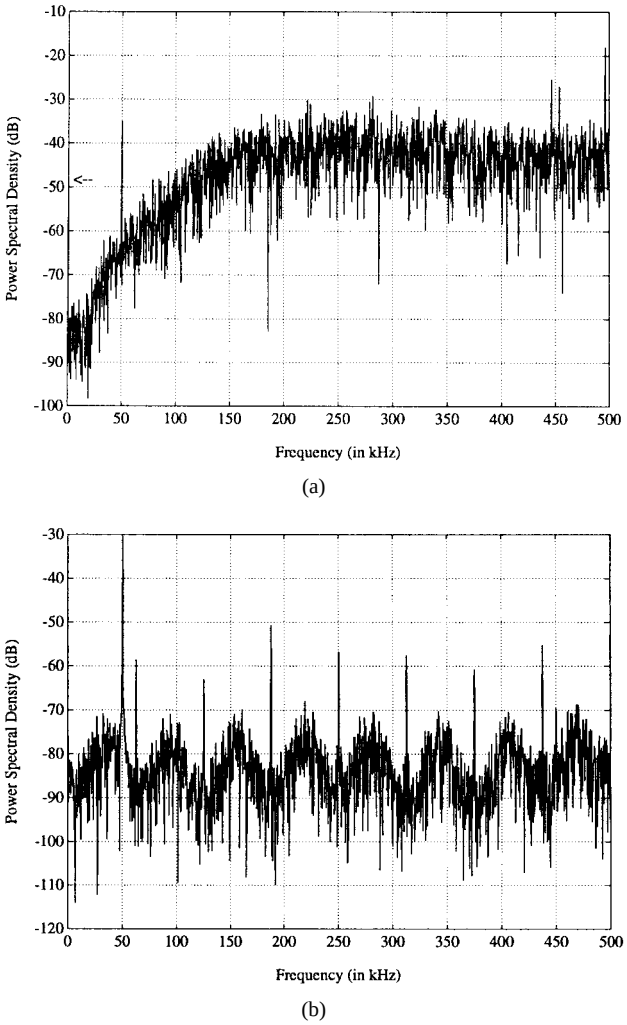

Fig. 5. Measured output of the $\Pi\Delta\Sigma$ A/D converter with offset at the input of the individual $\Delta\Sigma$ modulators. (a) Modulator output of first channel of the 16-channel $\Pi\Delta\Sigma$ modulator and (b) overall output of A/D converter.

B. Thermal Noise

An important design consideration in switched-capacitor implementations of $\Delta\Sigma$ A/D converters is the input-referred thermal noise. Assuming that the thermal noise due to the sampling capacitor C is the dominant noise source, the thermal noise power is given by

$$\sigma_{\text{th}}^2 = \frac{\alpha kT}{OSR \cdot C} \tag{6}$$

where α will vary depending on the implementation and is typically two, k is Boltzmann's constant, T is the absolute temperature, and OSR is the oversampling [7]. In the Nyquist-rate $\Pi\Delta\Sigma$ A/D converter, the input-referred thermal noise

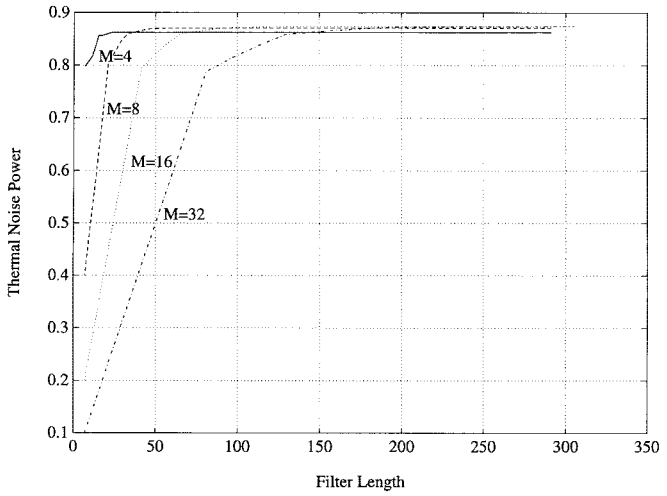

Fig. 6. Thermal noise output power of the $\Pi\Delta\Sigma$ A/D converter normalized to σ_{th}^2 versus filter length N.

power on each channel is

$$\sigma_{\text{th}}^2 = \frac{\alpha kT}{C}. \tag{7}$$

The total input thermal noise power is

$$\sigma_{\text{th,tot}}^2 = M\sigma_{\text{th}}^2 \sum_{n=0}^{N-1} h^2(n) \tag{8}$$

where $h(n)$ is the impulse response of the optimal digital filter and

$$\sum_{n=0}^{N-1} h^2(n) \approx \frac{1}{M} \tag{9}$$

therefore

$$\sigma_{\text{th,tot}}^2 \propto \sigma_{\text{th}}^2. \tag{10}$$

The thermal noise power (normalized to σ_{th}^2) at the output of the $\Pi\Delta\Sigma$ A/D converter implemented with second-order $\Delta\Sigma$ modulators with sufficiently long filters is approximately $0.85\sigma_{\text{th}}^2$. This result is independent of the number of channels as shown in Fig. 6. M times more noise is contributed by increasing the number of channels by M, however, the bandwidth of the filter is also reduced by a factor of $1/M$. Thus, a constant thermal noise is produced independent of the number of channels. This property holds for other-order modulators as well.

C. Operational Amplifier Requirements

Finite gain in the operational amplifiers causes leakage in the integrators [6]. When the $\Pi\Delta\Sigma$ A/D converter is implemented with second-order modulators, no appreciable reduction in the performance is obtained with op amp open-loop gains on the order of the product of the number of channels times the oversampling ratio. This is similar to the single modulator case where the gain must be on the order of the oversampling ratio. This is expected as the filter cutoff frequency is approximately $1/(M \cdot OSR)$ for the $\Pi\Delta\Sigma$ A/D converter and $1/OSR$ for the $\Delta\Sigma$ A/D converter.

As in the $\Delta\Sigma$ A/D converter design, nonlinear settling in the amplifiers degrades the performance which necessitates op amps that are not slew-rate limited. Similarly, the unity gain bandwidth required is a few times the clock frequency [6].

V. Design Implementation

A chip consisting of five second-order switched-capacitor modulators as shown in Fig. 7 was integrated in a 1.2-μm n-well CMOS process. The die microphotograph is shown in Fig. 8. A fully differential integrator is employed for its superior power-supply rejection and extended dynamic range. The capacitor values were chosen as $C_1 = 1$ pF and $C_2 = 2$ pF to achieve a thermal noise floor below 12 b. Each $\Delta\Sigma$ modulator consists of a Hadamard modulator at its input as shown in Fig. 7. The Hadamard modulation circuitry simply consists of transmission gates which either pass the differential signal or cross the inputs. The clocks controlling the Hadamard switches are the opposite clock phase as the $\Delta\Sigma$ modulator input sampling switches so that the settling of the Hadamard switches does not degrade the performance. The $\Delta\Sigma$ modulator is controlled by two-phase nonoverlapping clocks where the feedback voltage is sampled on $\phi 2$. Fully differential folded-cascode op amps with switched-capacitor common-mode feedback were used for the integrators in the $\Delta\Sigma$ modulators [10]. Table II lists the amplifier characteristics. A latched comparator as in [10] clocked on $\phi 2$ was used in this design.

The Hadamard sequence is generated off-chip and it controls the gates of the MOSFET switches on-chip. This allows combining any number of parallel channels in testing the architecture. The buffered output of each modulator connects to an output pin so that filtering and demodulation may be performed on the computer to compute the overall converter output. The voltage reference was also supplied off-chip.

To test the architecture, two chips were wired in parallel on a two-sided PC board. A Tektronix LV500 digital tester was used to supply the digital Hadamard sequences and collect the digital output data from each channel. The output from each channel's $\Delta\Sigma$ modulator was filtered, demodulated, and recombined. The Nyquist-rate eight-channel $\Pi\Delta\Sigma$ A/D converter output spectrum clocked at 320 kHz and with an input signal frequency of 160 kHz is shown in Fig. 9. Notice the "*bumps*" in the noise floor that result when the filtered channels are recombined. As the theory predicts, the eight-channel $\Pi\Delta\Sigma$ A/D converter achieved 27 dB of dynamic range as shown in Fig. 10. The signal overloads at approximately -6 dB which is similar to the conventional delta–sigma modulator.

Increasing the number of channels from two to four and from four to eight, an increase of 1.6 and 2.3 b, respectively, was obtained. For small numbers of channels, the increase in resolution will not exactly agree with the theory because the noise transfer function does not exactly match the theoretically assumed value of $(1 - z^{-1})^2$. To illustrate this point, the transfer function for the ideal transfer function with two zeros at dc and the measured output from the first channel are plotted in Fig. 11. For low numbers of channels, the noise power

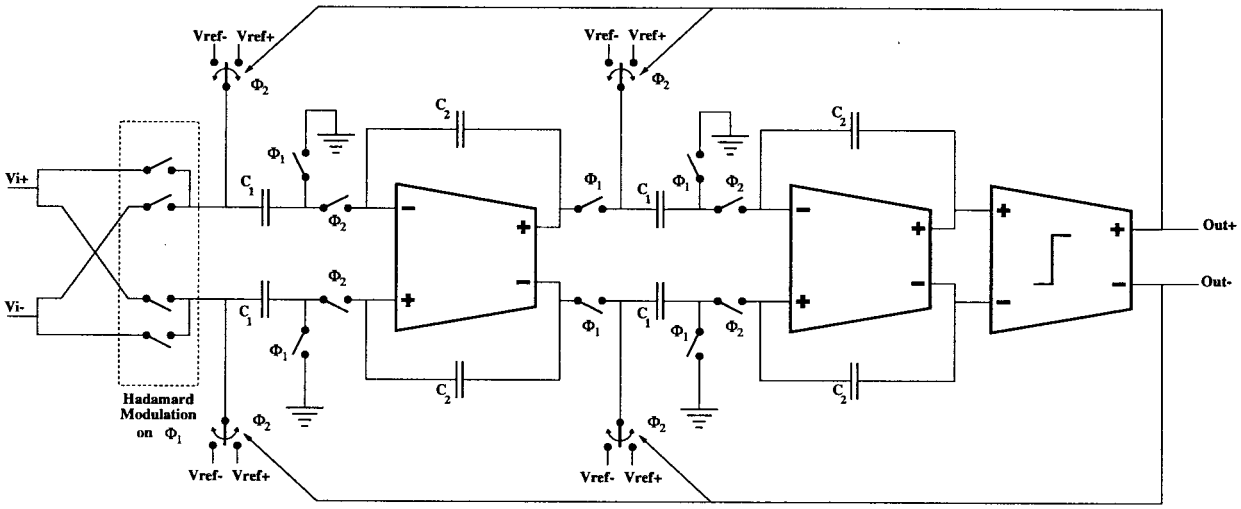

Fig. 7. Fully differential second-order delta–sigma modulator consisting of two-phase nonoverlapping clocks ϕ_1 and ϕ_2.

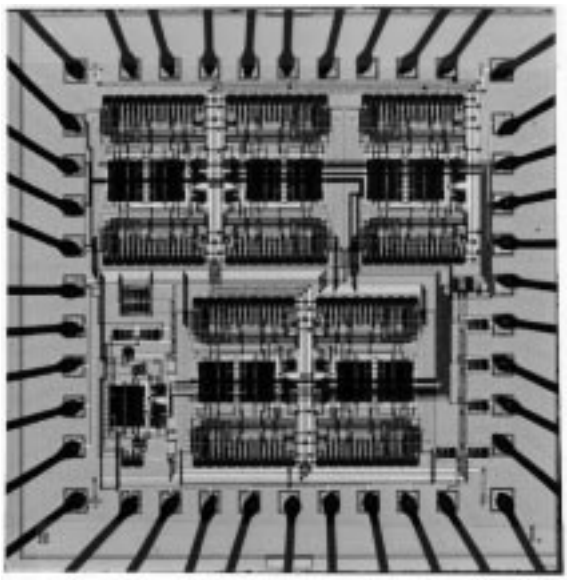

Fig. 8. Die microphotograph. Five second-order $\Delta\Sigma$ modulators are integrated on the die. Each modulator is 500 μm$\times$ 400 μm.

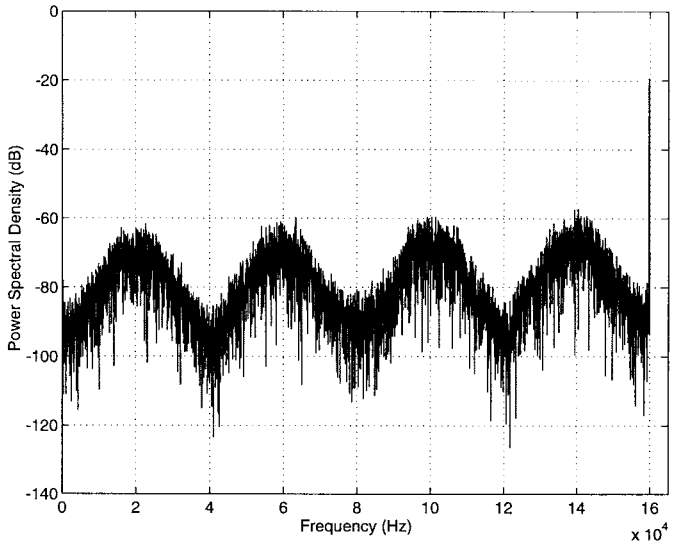

Fig. 9. Eight-channel $\Pi\Delta\Sigma$ A/D converter output spectrum with 320-kHz clock and 160-kHz input signal frequencies. The conversion bandwidth is 320 kHz.

TABLE II
FOLDED-CASCODE OPERATIONAL AMPLIFIER CHARACTERISTICS

Open loop gain	60 dB
Unity gain frequency	50 MHz
Power dissipation	9 mW
Settling time	3 ns
Slew rate	300 V/μs

in the two cases will be different as the two curves deviate at $f_s/4$. However, for higher numbers of channels and/or a high oversampling ratio, the performance of the $\Pi\Delta\Sigma$ A/D converter follows the theoretically predicted performance. It is important to note, however, that the simulated and measured performance are in agreement.

Combining oversampling with parallelism in the $\Pi\Delta\Sigma$ A/D converter offers another degree of freedom in the implementation. For a second-order $\Delta\Sigma$ modulator, the resolution increases by 2.5 b for every doubling in the oversampling ratio. The output spectrum for the eight-channel $\Pi\Delta\Sigma$ A/D converter with five times oversampling is shown in Fig. 12. In this plot the clock frequency is 1 MHz and the input signal is 3 kHz. The measured resolution is nearly 8.5 b with an input amplitude of -6 dB, and the full dynamic range is 9.5 b.

Using the integrated circuit prototype, four-channel and eight-channel $\Pi\Delta\Sigma$ A/D converters with three and five times oversampling were measured (Table III). The ideal performance is shown in Fig. 13. The optimal filters require that an odd oversampling ratio be used. For both the four- and eight-channel converters, with no oversampling and three times oversampling, the increase in resolution is 3.5 b. The increase in resolution obtained from three to five times oversampling is 1.8 b for four and eight channels.

The measurements presented here verify the operation of the parallel delta–sigma A/D converter without oversampling and with moderate oversampling. For the resolutions obtained in this implementation, errors due to channel mismatches do

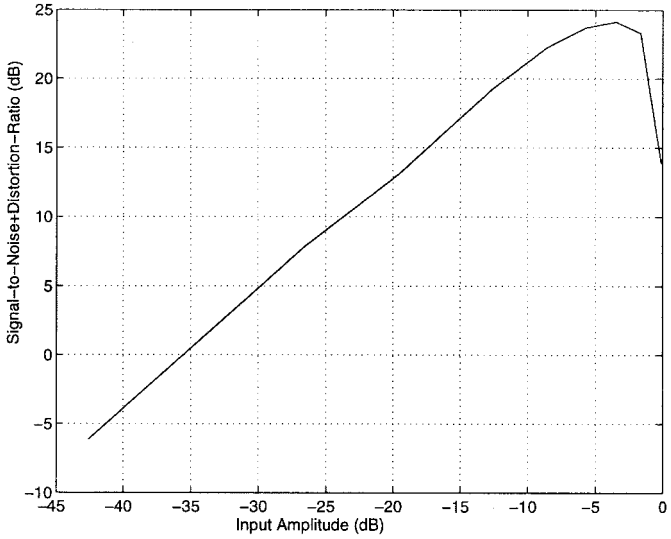

Fig. 10. Measured signal-to-(noise + distortion) ratio versus input amplitude (where 0 dB $= \Delta/2 = 2$ V) for the eight-channel $\Pi\Delta\Sigma$ A/D converter operating at the Nyquist rate.

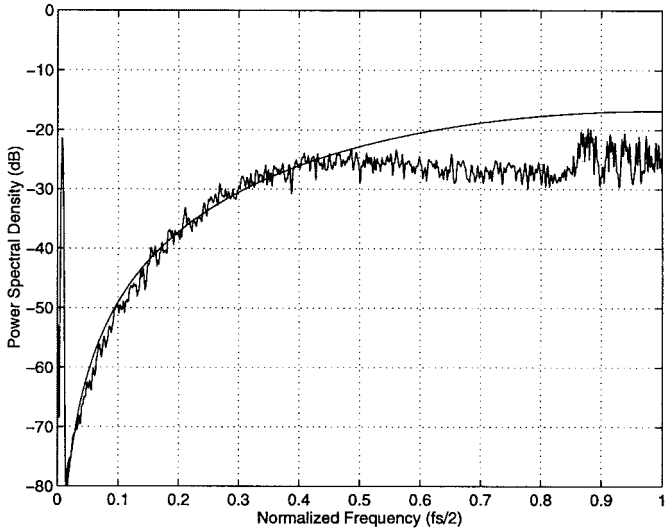

Fig. 11. Plot of second-order $\Delta\Sigma$ modulator quantization noise filter magnitude response normalized to half the sampling frequency. The upper curve is the ideal response and the lower curve is the response for a typical implementation. The markers indicate the -3 dB frequencies for the filters that follow the modulators. The marker labeled 0.44 corresponds to two channels, 0.22 corresponds to four channels, 0.11 corresponds to eight channels, and 0.05 corresponds to 16 channels.

not appear. Simulations show that for channel matching of 0.1%, 100 dB of spurious free dynamic range is obtained for four fourth-order delta–sigma A/D converters with ten times oversampling [8]. This architecture appears to be promising for combining both oversampling and parallelism to obtain high-speed and high-resolution conversion. Future research will focus on demonstrating this capability.

VI. Conclusion

This paper provides the first experimental demonstration of the $\Pi\Delta\Sigma$ A/D architecture. The unique design considerations of such a converter have been described and verified through

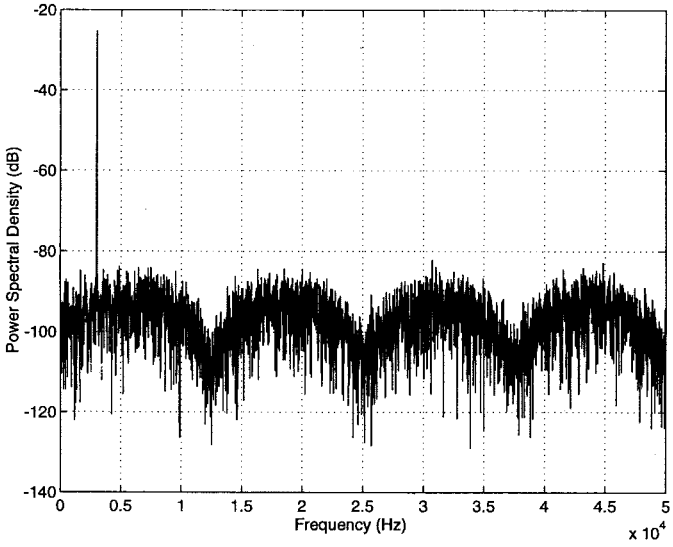

Fig. 12. Eight-channel $\Pi\Delta\Sigma$ A/D converter output spectrum with five-times oversampling. The clock frequency is 1 MHz, the input frequency is 3 kHz, and the conversion bandwidth is 200 kHz.

TABLE III
Measured Signal-to-Noise Ratio for the $\Pi\Delta\Sigma$ A/D Converter with an Oversampling Ratio of One, Three, and Five Times

OSR	4-Channels	8-Channels
One	11.1 dB	25.3 dB
Three	33.2 dB	45.8 dB
Five	43.8 dB	56.8 dB

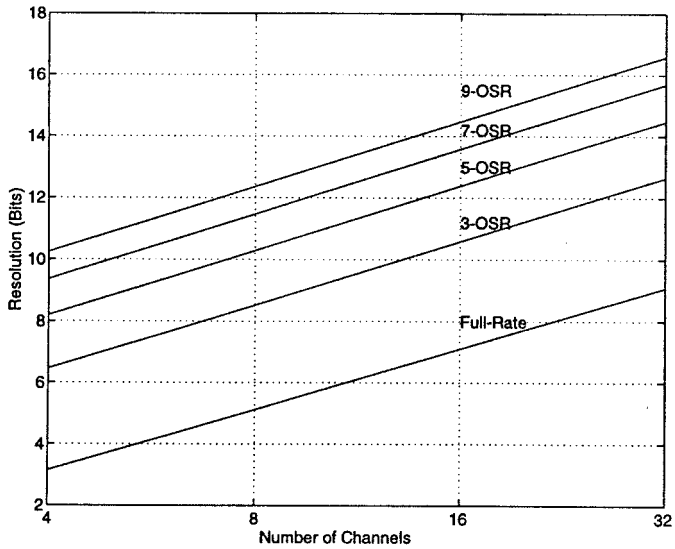

Fig. 13. Plot of resolution versus number of channels for the second-order $\Pi\Delta\Sigma$ A/D converter with various oversampling ratios.

measurements of prototypes. The theoretically predicted performance has been verified through an eight-channel $\Pi\Delta\Sigma$ A/D converter implementation where both oversampling up to a factor of five and no oversampling were used. In conventional $\Delta\Sigma$ A/D converters, the order of the modulator or the oversampling ratio can be adjusted to vary the speed and resolution of the conversion process. The $\Pi\Delta\Sigma$ A/D converter offers one more degree of freedom in the design of $\Delta\Sigma$

A/D converters: parallelism. This initial exploration into the design considerations of the $\Pi\Delta\Sigma$ A/D converter is a first step in the development of this architecture. Future research will investigate the combination of some oversampling with multiple channels.

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