SP 23.2: A ΔΣPLL for 14b 50kSample/s Frequency-to-Digital Conversion of a 10MHz FM Signal

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In wireless applications, digital signal processing is increasingly used in place of analog processing to improve reliability, reduce manufacturing cost, and allow programmability. Usually, the requisite A/D conversion is performed after the RF signal is down-converted to an intermediate frequency (IF) in the 0-100MHz range, and the demodulation is digital. Design simplifications, such as the avoidance of in-phase and quadrature analog processing, can often be achieved if the A/D conversion is above 5MHz, but in CMOS technology such systems are usually limited to about 12b precision [1, 2]. This key component of a CMOS frequency-to-digital converter (FDC), a device that simultaneously performs A/D conversion and frequency demodulation, in certain cases, promises to be an attractive alternative to conventional non-zero IF A/D conversion.

As shown in Figure 1, the FDC consists of a hard limiter, a ΔΣ phase-locked loop (ΔΣPLL), and a non-uniform to uniform decimation filter [3]. The ΔΣPLL estimates the instantaneous frequency deviation relative to 10MHz of the input signal from its zero crossings, and generates a 2b sequence consisting of the estimate plus 2nd-order highpass quantization noise. Like a ΔΣADC, the decimation filter removes the out-of-band quantization noise and downsamples to generate a high-precision digitized estimate of the desired signal. Performance is summarized in Table 1.

Viewed as an FM demodulator, the system is similar to a limiter-discriminator because it operates on the zero-crossings of the input signal. Although such discriminators are susceptible to out-of-band interferers, they are widely used in commercial receivers because of the availability of low-cost crystal and SAW filters centered at various convenient IF frequencies including 10MHz.

The ΔΣPLL functional diagram is shown in Figure 2. Two events control the timing: 1) transition of $x_r(t)$ from low to high, and 2) transition of the carry signal from low to high. The 4b counter is driven by an 80MHz external clock, and the carry signal goes high on its terminal count. In normal operation, output of the *XOR* gate goes high when $x_r(t)$ goes high. This switches the positive current source, "I_p", toward the capacitor until the carry signal goes high, at which time it is switched away from the capacitor. The negative current source, "I_n", is switched toward the capacitor for a fixed duration each time the carry signal goes high. Two 80MHz clock cycles after the carry signal goes high, the counter is loaded with a number obtained by filtering the ADC output by $2\text{-}z^{-1}$ and adding 9. This effectively sets the time until the next carry closing the feedback loop.

The switched current sources are the most critical components in the ΔΣPLL. Settling in <6ns without overshoot is required to ensure 14b FDC performance. A simplified diagram of the negative current source is shown in Figure 3. When I_n Pulse is high, M_3 and M_7 are off, so M_1 and M_2 act as a cascode current source of approximately 18μA . When I_n Pulse goes low, M_3 and M_4 act as a cascode current source of 20μA which causes the voltage at node 1 to rise to the point where M_2 is turned off. Transistors M_6-M_8 act as a clamping circuit that limits the voltage swing at node 1 to facilitate high-speed switching. Although a simpler switched current source could be obtained by replacing transistors M_3-M_8 by a single n-channel transistor, the circuit of Figure 3 offers the advantage that overshoot is eliminated.

As with most discrete-time PLLs, the ΔΣPLL provides output samples at non-uniform intervals. In the case of the ΔΣPLL, a simple digital interpolation can be used in conjunction with the decimation filtering to perform non-uniform to uniform decimation. As shown in Reference 3, aside from quantization noise and a well-defined constant, each output sample of the ΔΣPLL is equal to the difference between its sample time and the time of the previous sample. By accumulating output samples, it is straightforward to determine which pairs of adjacent output samples straddle the desired downsampling times. The decimation filter locates these points and performs a simple two-point interpolation on each pair (involving two multiplications at the downsampled rate) to determine the corresponding downsampled value.

High-level schematic diagrams of the two classes of measurements performed on the prototype ΔΣPLL are shown in Figure 4 along with power spectral density (PSD) plots of the corresponding measured data. The left PSD corresponds to the 2b output of the ΔΣPLL driven by a 9MHz sinusoid (i.e., a dc FM message signal). As expected, the plot is identical to that of a second-order ΔΣ modulator driven by a dc signal. The right PSD corresponds to the full FDC in which the ΔΣPLL is driven by an FM signal with 12kHz sinusoidal message signal and 500kHz frequency deviation. The decimation filter output rate is 50kSample/s. For this case, the measured signal to noise and distortion ratio (SINAD) is 86.4dB and the measured spurious-free dynamic range (SFDR) is 90.5dB.

In an ADC, the peak SINAD and SFDR are determined by increasing the amplitude of the input signal until the measured SINAD and SFDR reach their maximum values. In an FDC, the same measurements are performed except the frequency deviation of the input signal is increased instead of the amplitude. Figure 5 shows a plot of measured SINAD and SFDR values as functions of increasing frequency deviation. In each case, the input signal is an FM signal with a 12kHz sinusoidal message signal. The resulting peak SINAD and SFDR were 89.1dB and 94.3dB, respectively. In general, the peak SINAD and SFDR were found to depend somewhat on the choice of the frequency and offset of the message signal used to generate the FM input signal. This is not surprising as the output sample times of the ΔΣPLL are related to these quantities, so spurs that are out-of-band for some input signals end up in-band for others. In testing, worst-case input signals were sought. The resulting worst-case peak SINAD and SFDR are 85.1dB and 88.1dB, respectively. On the basis of measurements performed on numerous different input signals and different copies of the chip, conservative estimates of typical values of peak SINAD and SFDR are 86.4dB and 91.3dB, respectively. Additional measurements performed with two-tone message signals are consistent with these SINAD and SFDR values.

Acknowledgments:

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References:

[1] Song, M., Jet al., "A Fully-Integrated 5MHz-IF FM Demodulator," Proceedings of the IEEE Custom Integrated Circuits Conference, May, 1997.

[2] Jantzi, S., K. Martin, A. Sedra, "A Quadrature Bandpass SD Modulator for Digital Radio," ISSCC Digest of Technical Papers, pp. 216-217, Feb., 1997.

[3] Galton, I., "Analog-Input Digital Phase-Locked Loops for Precise Frequency and Phase Demodulation," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 42, no. 10, pp. 621-630, Oct., 1995.

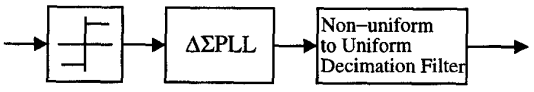

Figure 1: The ΔΣ frequency-to-digital converter high-level view.

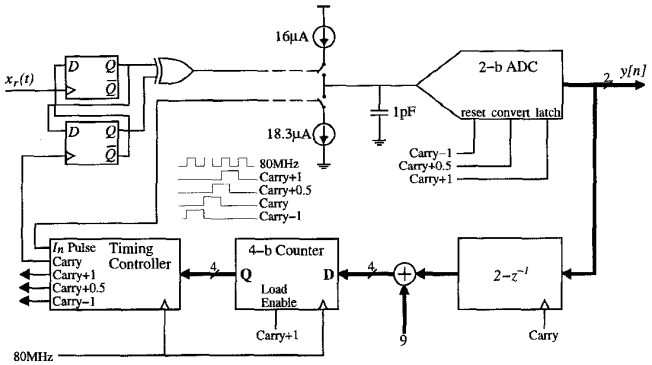

Figure 2: The ΔΣPLL functional diagram.

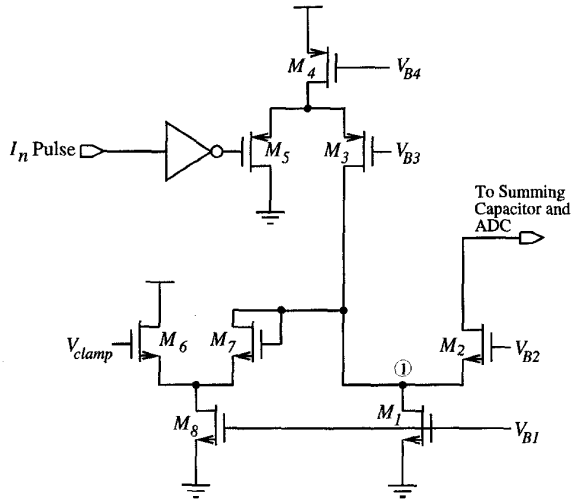

Figure 3: A simplified schematic diagram of the negative switched current source.

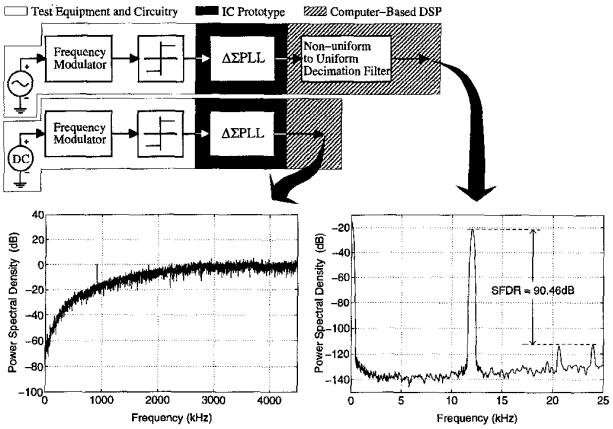

Figure 4: Measurement schematic and PSD plots of representative measured data.

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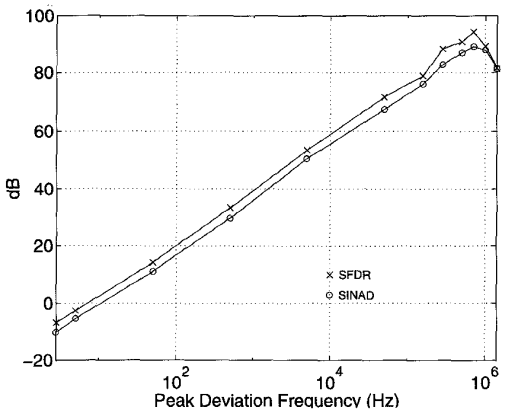

Figure 5: Measured SINAD and SFDR versus frequency deviation (i.e., message signal amplitude).

Figure 6: See page 465.

Technology	0.6μm single-poly CMOS
Input no-overload range	8.9MHz to 10.0MHz
FDC output sample-rate	50kSample/s
Worst-case FDC SINAD	85.1dB
Worst-case FDC SFDR	88.1dB
Typical FDC SINAD	86.4dB
Typical FDC SFDR	91.3dB
External clock frequency	80MHz
Supply voltage	5V
Power dissipation (analog)	3mW
Power dissipation (digital)	32mW
Total power dissipation	35mW
Die size	4mm^2
Active area	0.6mm^2

Table 1: Measurement summary.

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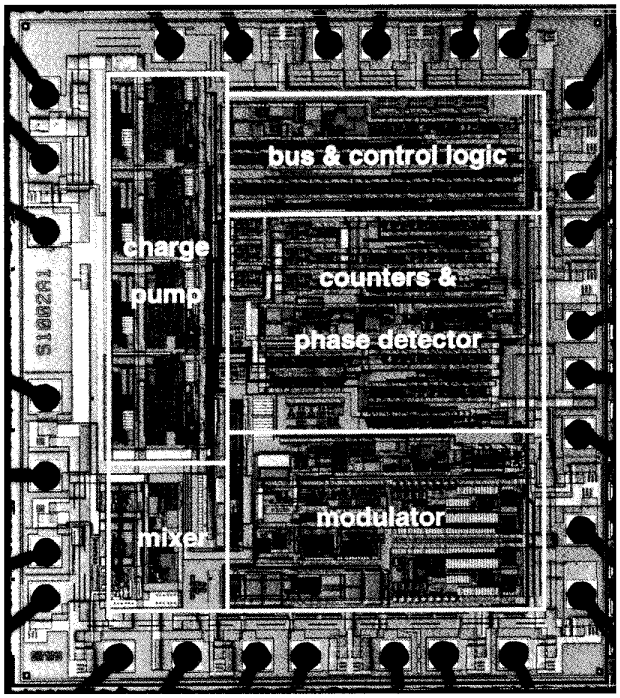

Figure 7: Chip micrograph.

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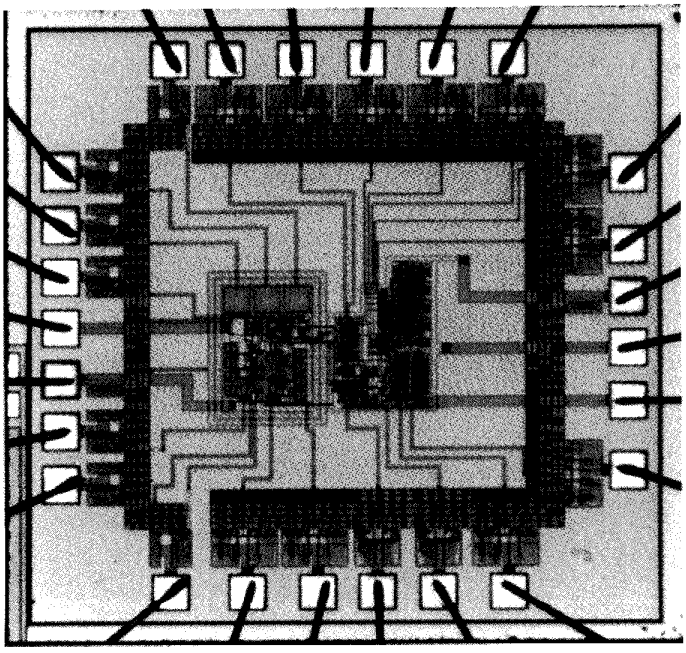

Figure 6: Die micrograph.