YIELD ESTIMATION OF A FIRST-ORDER NOISE-SHAPING D/A CONVERTER

Henrik T. Jensen Ian Galton

Department of Electrical & Computer Engineering
UNIVERSITY OF CALIFORNIA, SAN DIEGO, La Jolla, CA 92093-0407, USA.
htjensen@ece.ucsd.edu galton@ece.ucsd.edu

ABSTRACT

This paper presents results that allow for a yield estimation analysis of a particular 1st-order noise-shaping digital-to-analog converter. While various dynamic element matching techniques for noise-shaping DACs have recently been proposed and their efficiency in $\Delta\Sigma$ data converter applications demonstrated with simulation data, no work that allows for an exact theoretical prediction of the noise-shaping performance has been published so-far. As the main result of this paper, the power spectral density (PSD) of the DAC noise of a 1st-order noise-shaping DAC can be predicted and used to generate yield estimation data of the power of the signal-band DAC noise given knowledge of the statistics of the static DAC-element errors.

1. INTRODUCTION

As is well-known, mismatches in the analog output levels cause conventional multi-bit DACs employed in $\Delta\Sigma$ data converters to introduce *DAC noise* that resides in the signal-band and thus drastically reduce the overall conversion precision compared to ideal performance. A number of investigators have recently proposed multi-bit *noise-shaping* DAC architectures in an on-going effort to develop practical multi-bit DACs for use in $\Delta\Sigma$ data converters. By moving most of the DAC noise away from the signal-band, noise-shaping DACs do not significantly deteriorate the performance of the $\Delta\Sigma$ data converters. While all publications of proposed noise-shaping DAC architectures have presented simulation data that indicate promising noise-shaping properties, no work that theoretically quantifies the performance has been published previously.

The results of this paper allow for a theoretical prediction of the PSD of the DAC noise of the 1st-order noise-shaping DAC proposed in [1]. Specifically, a 2-bit version of the DAC employed in a 2nd-order $\Delta\Sigma$ADC with a 2-bit quantizer is considered in detail. The performance of the 1st-order noise-shaping DAC and the $\Delta\Sigma$ADC is demonstrated with simulation data, and a comparison between simulated and predicted PSDs is provided. IC fabrication yield estimation data of the power of the DAC noise computed by integrating the predicted PSD of the DAC noise over the signal-band is presented. This data is subsequently used to generate an IC fabrication yield estimation of the overall conversion precision of the 2nd-order $\Delta\Sigma$ADC.

2. THE DAC AND $\Delta\Sigma$ADC ARCHITECTURES

To first review the architecture of the 1st-order noise-shaping DAC proposed in [1], consider the 2-bit version shown in Fig. 1. The DAC input, $x_D[n]$, is a sequence of unsigned 2-bit binary numbers in the range 0 through 3. The DAC consists of 2 layers of digital devices, each device referred to as a *switching block*, followed by 4 one-bit DACs, each referred to as a *unit DAC-element*, and an analog output summing node to generate the DAC output $y_D[n]$. Each switching block is labeled $S_{k,m}$, where k denotes the layer number and m denotes the position of the switching block in the layer. The signal-processing details of the switching block are shown in Fig. 2a. It has one $k+1$-bit input, $x_{k,r}[n]$, and two k-bit outputs, $x_{k-1,2r-1}[n]$ and $x_{k-1,2r}[n]$, respectively. The outputs are formed according to

$$x_{k-1,2r-1}[n] = \frac{1}{2}(x_{k,r}[n] + s_{k,r}[n])$$

and

$$x_{k-1,2r}[n] = \frac{1}{2}(x_{k,r}[n] - s_{k,r}[n]),$$

where $s_{k,r}[n]$ is a *switching sequence* generated according to the signal-processing algorithm of Fig. 2b. The structure of Fig. 2b closely resembles a 1st-order $\Delta\Sigma$ modulator with no input signal, except for the LSB multiplier and the *dithered hard limiter*. The dithered hard limiter operates according to

$$v_{k,r}[n] = \begin{cases} 1, & \text{if } u_{k,r}[n] = 1; \\ -1, & \text{if } u_{k,r}[n] = -1; \\ r_{k,r}[n], & \text{if } u_{k,r}[n] = 0; \end{cases}$$

where $v_{k,r}[n]$ is the output of the device, $u_{k,r}[n]$ is the input of the device, and $r_{k,r}[n]$ is a random ± 1 sequence that is white, independent of $x[n]$, and uncorrelated with the $r_{k,r}[n]$ sequences in the other switching blocks. A hardware-efficient gate-level implementation of the signal processing algorithms of Fig. 2 is given in [2].

Fig. 3a shows the functional details of the 2nd-order $\Delta\Sigma$ADC. The analog input and the digital output are denoted $x[n]$ and $y[n]$, respectively. The coarsely quantized $\Delta\Sigma$ADC output is generated by a 4-level uniform quantizer with quantization levels 0, 1, 2, and 3. For the purposes of this paper, $x[n]$ is assumed to be amplitude-limited such that the quantizer operates within the no-overload range. The 2-bit 1st-order noise-shaping DAC of Fig. 1 is employed in the feed-back path of the $\Delta\Sigma$ modulator loop.

3. PERFORMANCE DETAILS

The unit DAC-elements of the noise-shaping DAC operate according to

$$y_r[n] = \begin{cases} 1 + e_{h_r}, & \text{if } x_r[n] = 1; \\ e_{l_r}, & \text{if } x_r[n] = 0; \end{cases}$$

1997 IEEE International Symposium on Circuits and Systems

0-7803-3583-X/97 $10.00 ©1997 IEEE

where $y_r[n]$ denotes the analog output of the r^{th} unit DAC-element, and e_{h_r} and e_{l_r} are errors in the analog output levels. The errors are assumed to be time-invariant, but otherwise arbitrary, and are referred to as *static DAC-element errors.*

As shown in [2], interconnecting the switching blocks and unit DAC-elements in the network of Fig. 1 results in a DAC for which $y_D[n] = x_D[n]$ in the absence of static DAC-element errors. However, with non-zero static DAC-element errors, the DAC output has the form

$$y_D[n] = \alpha x_D[n] + \beta + e_D[n], \tag{1}$$

where α is a constant gain, β is a DC offset, and $e_D[n]$ is the DAC noise. Formulae for α and β are given in [2]; here it suffices to know that they depend only on the static DAC-element errors. The DAC of Fig. 1 achieves *first-order* noise-shaping by decorrelating $e_D[n]$ from $x_D[n]$ and spectrally shaping $e_D[n]$ such that its PSD ideally resembles that of white noise filtered by the highpass filter $H(z) = 1 - z^{-1}$.

The quantization noise, $e_Q[n]$, introduced by the quantizer is commonly modeled as an additive white-noise process, uncorrelated with $x[n]$. Applying this model, it follows that the signal-processing equivalent of the $\Delta\Sigma$ADC of Fig. 3a is given by Fig. 3b, where the signals $x[n]$, $e_Q[n]$, and $e_D[n]$ are uncorrelated. With a linear systems analysis it can be shown that the transfer functions between the $\Delta\Sigma$ADC output $y[n]$ and the signals $x[n]$, $e_Q[n]$, and $e_D[n]$, are given by

$$\frac{Y(z)}{X(z)} = N_X(z)D(z) = z^{-1}D(z), \tag{2}$$

$$\frac{Y(z)}{E_Q(z)} = N_Q(z)D(z) = (1 - z^{-1})^2 D(z), \tag{3}$$

and

$$\frac{Y(z)}{E_D(z)} = N_D(z)D(z) = (z^{-1} - 2)z^{-1}D(z), \tag{4}$$

respectively, where the term

$$D(z) = [1 + 2(\alpha - 1)z^{-1} + (1 - \alpha)z^{-2}]^{-1} \tag{5}$$

can be viewed as a distortion of the ideal transfer functions $N_X(z), N_Q(z)$, and $N_D(z)$, resulting from a non-unity value of α. The importance of $D(z)$ will be considered in the next section.

It follows from the above that both of the noise-sources $e_Q[n]$ and $e_D[n]$ contribute to the *overall* conversion error at the output of the $\Delta\Sigma$ADC. This error will subsequently be referred to as the *$\Delta\Sigma$ADC noise*, $e_{ADC}[n]$. It follows from (2) and (5) that the $\Delta\Sigma$ADC noise can be written in the form

$$e_{ADC}[n] = y[n]+2(\alpha-1)y[n-1]+(1-\alpha)y[n-2]-x[n-1]. \tag{6}$$

While this particular form is not very useful for a statistical analysis, it does provide a simple formula to compute $e_{ADC}[n]$ for simulation purposes, as will be demonstrated shortly.

For a statistical analysis of $e_{ADC}[n]$, notice that (3) and (4) imply that the PSD of $e_{ADC}[n]$ is given by

$$\begin{aligned} S_{e_{ADC}e_{ADC}}(e^{j\omega}) =& S_{e_Qe_Q}(e^{j\omega})|N_Q(e^{j\omega})D(e^{j\omega})|^2 \\ &+ S_{e_De_D}(e^{j\omega})|N_D(e^{j\omega})D(e^{j\omega})|^2 \end{aligned} \tag{7}$$

where $S_{e_Qe_Q}(e^{j\omega})$ and $S_{e_De_D}(e^{j\omega})$ denote the PSDs of $e_Q[n]$ and $e_D[n]$, respectively. For the model of $e_Q[n]$ used in Fig. 3b,

$$S_{e_Qe_Q}(e^{j\omega}) = \frac{\Delta^2}{12}, \tag{8}$$

where Δ is the step-size of the quantizer (in Fig. 3, $\Delta = 1$). To evaluate (7), it remains to develop an expression for $S_{e_De_D}(e^{j\omega})$. This is done in detail in [3]; for the purposes of this presentation, the core of the derivation from [3] will be stated without rigorous proofs, although the theoretical results will be supported by simulations.

In accordance with the usual definitions, let the statistical auto-correlation of a sequence $x[n]$ be given by

$$R_{xx}[n, m] = \mathrm{E}\{x[n]x[n + m]\},$$

where $\mathrm{E}\{\cdot\}$ denotes the statistical expectation operator, and let the time-average autocorrelation of $x[n]$ be given by

$$\overline{R}_{xx}[m] = \lim_{P\to\infty} \frac{1}{P} \sum_{n=1}^{P} x[n]x[n + m].$$

As shown in [2], the DAC noise has the form

$$e_D[n] = \sum_{k=1}^{2} \sum_{r=1}^{2^{2-k}} \Delta_{k,r} s_{k,r}[n]. \tag{9}$$

It follows that

$$\begin{aligned} R_{e_De_D}[n, m] &= \mathrm{E}\{e[n]e[n + m]\} \\ &= \mathrm{E}\{(\sum_{k=1}^{2} \sum_{r=1}^{2^{2-k}} \Delta_{k,r} s_{k,r}[n])(\sum_{k=1}^{2} \sum_{r=1}^{2^{2-k}} \Delta_{k,r} s_{k,r}[n + m])\}. \end{aligned}$$

As shown in [3], the switching sequences, $s_{k,r}[n]$, are uncorrelated with each other, and thus

$$R_{e_De_D}[n, m] = \sum_{k=1}^{2} \sum_{r=1}^{2^{2-k}} \Delta_{k,r}^2 R_{s_{k,r}s_{k,r}}[n, m].$$

The autocorrelations of the switching sequences within each layer are identical [3], i.e., $R_{s_{k,r}s_{k,r}}[n, m] = R_k[n, m]$, and it follows that

$$R_{e_De_D}[n, m] = \sum_{k=1}^{2} \gamma_k R_k[n, m],$$

where

$$\gamma_k = \sum_{r=1}^{2^{2-k}} \Delta_{k,r}^2. \quad (10)$$

Then, as argued in [3],

$$\overline{R}_{e_D e_D}[m] = \sum_{k=1}^{2} \gamma_k \overline{R}_k[m] \quad (11)$$

with probability 1. In (11), $\overline{R}_k[m]$ depends only on $x_D[n]$, and a method for calculating $\overline{R}_k[m]$ is derived in [3]. The PSD of the DAC noise is then given by the Fourier-transform of (11), i.e.,

$$S_{e_D e_D}(e^{j\omega}) = \sum_{k=1}^{2} \gamma_k S_k(e^{j\omega}). \quad (12)$$

To summarize, the above results allow for a theoretical computation of the PSDs of the DAC noise and the $\Delta\Sigma$ADC noise.

Simulated performance of the 2nd-order $\Delta\Sigma$ADC of Fig. 3a is presented in Fig. 4. Each plot in the figure shows the PSD in dB relative to Δ^2 of a particular signal of the $\Delta\Sigma$ADC with a sinusoidal excitation. The frequency scales are normalized such that unity corresponds to half the sample rate of the $\Delta\Sigma$ADC output. The static DAC-element errors of the 2-bit DAC were chosen randomly from a normal distribution with a standard deviation of 1%. Specifically, Fig. 4a shows the $\Delta\Sigma$ADC output $y[n]$, Fig. 4b shows the DAC noise $e_D[n]$ formed using (1), Fig. 4c shows the $\Delta\Sigma$ADC noise $e_{ADC}[n]$ formed using (6) and plotted against a logarithmic frequency scale, and Fig. 4d shows $e_D[n]$ plotted against a logarithmic frequency scale.

The data of Fig. 4 clearly demonstrate spectral shaping of $e_{ADC}[n]$ and $e_D[n]$, respectively. From Fig. 4d, it is seen that the DAC noise exhibits 1st-order behavior, i.e., a decrease by 6 dB of the noise-floor per octave decrease in frequency. Because of a considerable difference in the power-levels at high frequencies between $e_Q[n]$ and $e_D[n]$, the $\Delta\Sigma$ADC noise of Fig. 4c exhibits both 1st-order and 2nd-order behavior. Specifically, while $e_Q[n]$ and $e_D[n]$ contribute with comparable powers at frequencies around $\omega_c = 10^{-2}$, the $\Delta\Sigma$ADC noise exhibits dominant 1st-order behavior for frequencies less than ω_c and dominant 2nd-order behavior for frequencies higher than ω_c.

Fig. 5 presents the theoretically computed PSDs of the $\Delta\Sigma$ADC noise and the DAC noise. Fig. 5a shows $e_{ADC}[n]$ as computed using (7), and Fig. 5b shows $e_D[n]$ as computed using (12). The plots are in agreement with the simulation data of Fig. 4c and Fig. 4d, respectively.

4. CONVERSION PRECISION

A standard measure of the $\Delta\Sigma$ADC conversion precision is the power of the $\Delta\Sigma$ADC noise with the restriction that the signal component of the $\Delta\Sigma$ADC output $y[n]$ be an undistorted version of the $\Delta\Sigma$ADC input $x[n]$. As found in the previous section, $x[n]$ is subjected to the linear distortion $D(z)$ given by (5), whose deviation from unity depends only on α. For practical values of α, the effects of $D(z)$ on the $\Delta\Sigma$ADC conversion precision is vanishingly small, but it will be taken into account here for completeness. From (7) it follows that power of the $\Delta\Sigma$ADC noise residing in the signal-band *after* signal equalization is given by

$$P_{e_{ADC}} = P_{e_D} + \frac{1}{2\pi} \int_{-\frac{\pi}{N}}^{\frac{\pi}{N}} S_{e_Q e_Q}(e^{j\omega}) |N_Q(e^{j\omega})|^2 \, d\omega \quad (13)$$

where N denotes the oversampling ratio, and P_{e_D} denotes the power of the DAC noise residing in the signal-band after signal equalization. From (4), it follows that

$$P_{e_D} = \frac{1}{2\pi} \int_{-\frac{\pi}{N}}^{\frac{\pi}{N}} S_{e_D e_D}(e^{j\omega}) |N_D(e^{j\omega})|^2 \, d\omega. \quad (14)$$

5. YIELD ESTIMATION

With knowledge of the statistical distribution of the static DAC-element errors, (13) and (14) allow for an IC fabrication yield estimation of the $\Delta\Sigma$ADC conversion precision and the power of the signal-band DAC noise, respectively. The IC yield estimation procedure used in the following is based upon the idea of computing a large number of samples of the parameter of interest for a given level of static DAC-element errors, thereby generating data that closely resemble the corresponding statistical distribution of the parameter.

An example of yield estimation data of P_{e_D} is shown in Fig. 6. Specifically, the figure shows P_{e_D} in dB relative to Δ^2 of the 2-bit DAC as a function of N and the static DAC-element errors. The oversampling ratio ranged from 16 to 512, and the static DAC-element errors were chosen randomly from a normal distribution with a standard deviation ranging from 0.05% to 2%. Fig. 6a and Fig. 6b show the largest of the smallest 95% and 5% values, respectively. For example, with $N = 128 = 2^7$ and static DAC-element errors with a standard deviation of 1%, the data of Fig. 6a predicts that 95% of all 2-bit DACs have signal-band noise powers less than -89.2 dB, while the data of Fig. 6b predicts that merely 5% of all 2-bit DACs have signal-band noise powers less than -102.6 dB. Thus, 90% of all DACs satisfy $-102.6 \text{ dB} \leq P_{e_D} \leq -89.2 \text{ dB}$.

Yield estimation data of the $\Delta\Sigma$ADC conversion bit-precision is shown in Fig. 7. For the same example as in the above, the data of Fig. 7a predicts that 95% of all 2nd-order $\Delta\Sigma$ADCs have conversion precisions less than 14.8 bits, while the data of Fig. 7b predicts that merely 5% of all 2nd-order $\Delta\Sigma$ADCs have conversion precisions less than 13.0 bits. Thus, 90% of all 2nd-order $\Delta\Sigma$ADCs provide a conversion precision of greater than 13.0 bits, but less than 14.8 bits.

6. CONCLUSION

Novel results that allow for a theoretical computation of the PSD of the DAC noise of the 1st-order noise-shaping DAC originally proposed in [1] have been presented. The results have been applied in a detailed performance analysis of a 2nd-order $\Delta\Sigma$ADC employing a 2-bit version of the DAC. It has been demonstrated how knowledge of the statistics of the static DAC-element errors can be used to generate IC fabrication yield estimation data of the power of the DAC noise and the overall conversion precision of the $\Delta\Sigma$ADC.

REFERENCES

1. I. Galton, "A hardware-efficient noise-shaping D/A converter," *Proceedings of the IEEE International Symposium on Circuits and Systems,* May, 1996.
2. I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters," *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing,* accepted for publication.
3. H.T. Jensen, I. Galton, "Yield estimation of a second-order ΔΣADC employing a noise-shaping DAC," *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing,* in preparation.

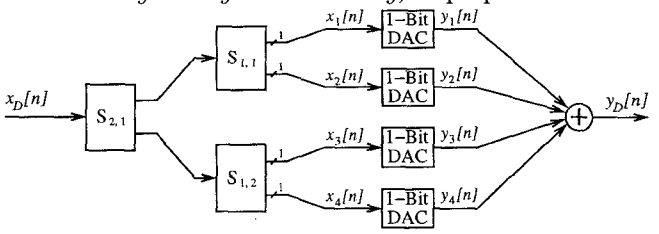

Figure 1: The 2-bit noise-shaping DAC.

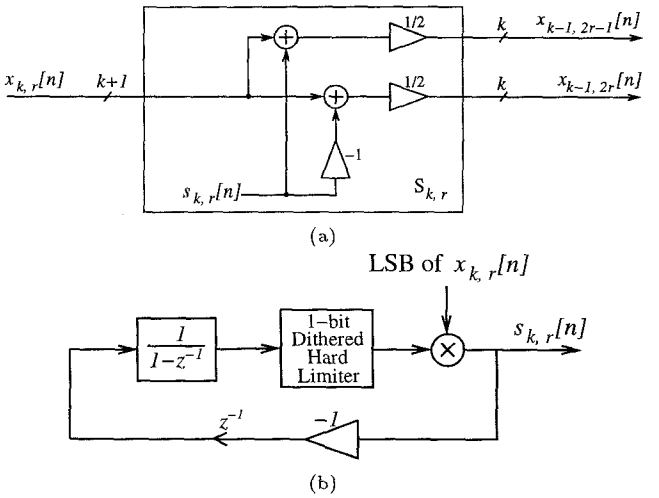

Figure 2: (a) The switching block $S_{k,r}$. (b) Generation of the switching sequence $s_{k,r}[n]$.

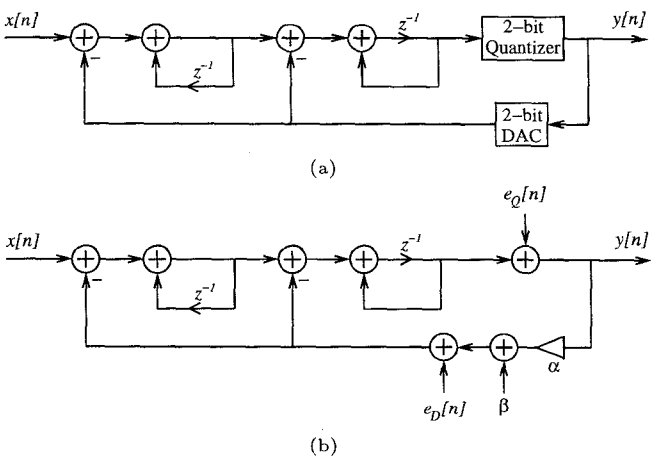

Figure 3: (a) The second-order ΔΣADC and (b) its signal-processing equivalent.

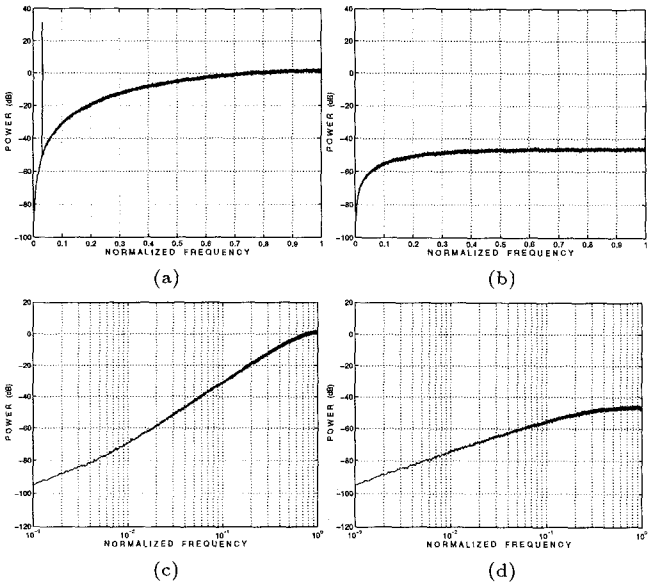

Figure 4: (a), (b), (c), and (d) Simulated PSDs.

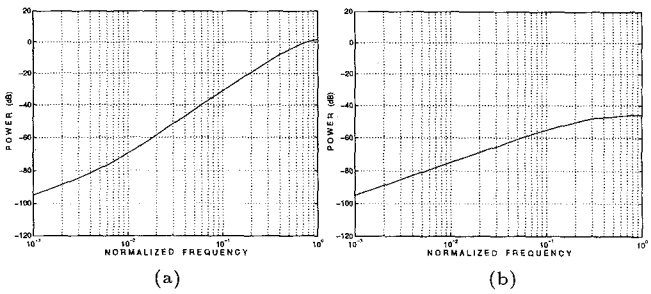

Figure 5: (a) and (b) Theoretical PSDs.

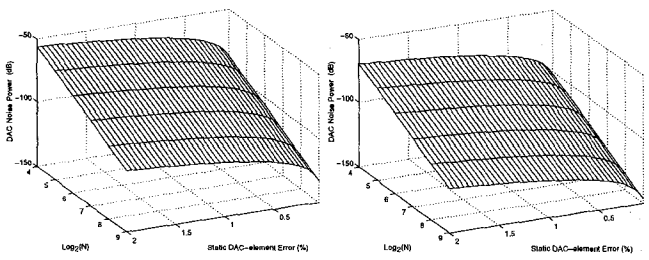

Figure 6: (a) and (b) Yield estimation data.

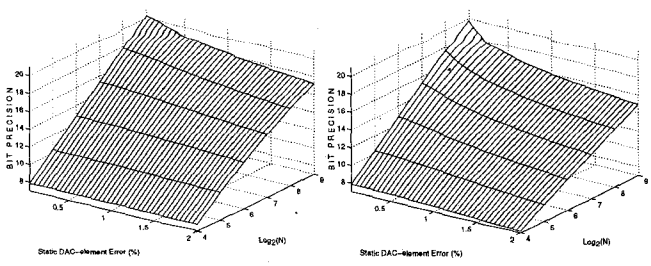

Figure 7: (a) and (b) Yield estimation data.