

# Oversampling Parallel Delta-Sigma Modulator A/D Conversion

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**Abstract**—Conventional delta-sigma analog-to-digital converters ( $\Delta\Sigma$ ADC's) are widely used in low-bandwidth applications such as high-fidelity audio processing because they offer high-precision conversion yet are amenable to implementation using fine-line VLSI processes optimized for digital circuitry. However, their oversampling requirement so far has prevented their widespread application to higher bandwidth applications such as video processing. This paper extends a recently developed delta-sigma ADC architecture called the pi-delta-sigma ADC ( $\Pi\Delta\Sigma$ ADC) that consists of multiple  $\Delta\Sigma$  modulator channels operating in parallel without time-interleaving. The extension developed in this paper allows for oversampling to be combined with parallelism such that an  $M$ -channel system with an oversampling ratio of  $N$  can achieve a conversion performance close to that of a conventional  $\Delta\Sigma$ ADC with an oversampling ratio of  $M \times N$ . Thus, for a given conversion precision, the architecture offers relaxed oversampling relative to conventional  $\Delta\Sigma$ ADC's in return for increased analog circuit area. Moreover, as will be shown, the  $\Pi\Delta\Sigma$ ADC retains much of the robustness of conventional  $\Delta\Sigma$ ADC's with respect to nonideal circuit behavior.

## I. INTRODUCTION

**I**N APPLICATIONS REQUIRING precise analog-to-digital (A/D) conversion with bandwidths less than a few megahertz, delta-sigma analog-to-digital converters ( $\Delta\Sigma$ ADC's) have enjoyed widespread application [1]. Their popularity derives from their reduced analog processing and relaxed sensitivity to analog circuit errors relative to other A/D conversion approaches. These advantages come at the expense of a relatively large amount of digital processing and the requirement that much of the circuitry must run at clock speeds that are significantly higher than the A/D conversion rate. These tradeoffs make them particularly well-suited for implementation in VLSI processes optimized for digital circuitry wherein analog accuracy tends to be sacrificed in favor of increased circuit density and speed.

Typically,  $\Delta\Sigma$ ADC's consist of a  $\Delta\Sigma$  modulator followed by a decimation filter. The  $\Delta\Sigma$  modulator samples the input signal at many times the Nyquist rate—a process referred to as *oversampling*—and performs very coarse A/D conversion on the resulting narrow-band sequence. Through the use of coarse D/A conversion and feedback, the quantization error introduced by the coarse A/D converter is spectrally shaped—a process referred to as *quantization noise shaping*—so that its power resides primarily outside the signal band. The decima-

tion filter removes the out-of-band portion of the quantization error and reduces the output rate to the Nyquist rate of the input signal.

Oversampling, in conjunction with quantization noise shaping and decimation filtering, thus results in the effect of high-precision A/D conversion despite the use of coarse A/D and D/A converters. In particular, 1 b A/D and D/A converters are often used which have the added benefit that static errors in their analog levels only affect the gain and offset of the overall system. Moreover, other types of error originating from nonideal circuit behavior such as analog circuit noise are at least partially removed by the decimation filter. Oversampling also permits the use of simple, low-order analog antialiasing filters because much of the required antialiasing functionality can be included in the digital decimation filter.

The primary drawback is that oversampling requires the  $\Delta\Sigma$  modulator and part of the decimation filter to operate at a significantly higher clock-rate than the desired A/D conversion rate. Therefore, the maximum A/D conversion rate is usually much lower than the maximum clock-rate for a given circuit technology. Most approaches to reducing the oversampling requirement have involved either increasing the order of the  $\Delta\Sigma$  modulator so as to improve its noise-shaping capability, increasing the number of coarse A/D converter bits, or a combination thereof. Unfortunately, increasing the order of the  $\Delta\Sigma$  modulator without increasing the number of coarse A/D converter bits generally results in systems that are only marginally stable and have reduced usable input ranges [2], [3] or that are sensitive to component matching errors [4]–[6]. Similarly, increasing the number of coarse A/D converter bits generally gives rise to systems that are highly sensitive to D/A converter errors in the  $\Delta\Sigma$  modulator feedback paths [1], [4].

Another approach to reducing the oversampling requirement is to operate multiple  $\Delta\Sigma$  modulator channels in parallel. To date, two different classes of parallel  $\Delta\Sigma$ ADC's have been proposed. One class is based on *time interleaving* wherein the input signal is sampled at the full rate, but most of the  $\Delta\Sigma$  modulator processing is performed by  $M$  coupled channels that each operate at an  $M$ th of the full rate [7], [8]. Although this does not eliminate the need for a high-rate sample-and-hold circuit, it does relax the speed requirements for much of the circuitry by a factor of  $M$ . The parallel  $\Delta\Sigma$ ADC's in the other class—referred to as  $\Pi\Delta\Sigma$ ADC's—avoid the oversampling requirement altogether through the use of multiple nontime-interleaved  $\Delta\Sigma$  modulator channels that process Hadamard modulated versions of the input signal sampled at the Nyquist rate [9], [10]. As shown in [9], in addition to

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avoiding oversampling the approach retains many of the advantages associated with conventional  $\Delta\Sigma$ ADC's. Its primary drawback is that it requires significantly more circuit area than the conventional  $\Delta\Sigma$ ADC. Moreover, although it eliminates the problems associated with oversampling, it also eliminates some of its benefits such as the reduced anti-aliasing filter requirement and attenuation of out-of-band circuit noise.

This paper presents an extension of the  $\Pi\Delta\Sigma$ ADC that allows for oversampling as a means of mitigating the above-mentioned drawbacks. As will be shown, with the proper choice of Hadamard modulation and filtering, an  $M$ -channel system with  $N$ -fold oversampling performs close to that of a conventional  $\Delta\Sigma$ ADC with  $M \times N$ -fold oversampling. For example, a four-channel, tenfold oversampling  $\Pi\Delta\Sigma$ ADC with fourth-order  $\Delta\Sigma$  modulators is considered in detail and shown to have a theoretical conversion precision of 18 b. In contrast, to obtain this precision using a conventional fourth-order  $\Delta\Sigma$ ADC would require approximately thirty-sixfold oversampling. Furthermore, the digital processing required for the example  $\Pi\Delta\Sigma$ ADC has about the same complexity as that required for the corresponding  $\Delta\Sigma$ ADC, and the two systems are similarly robust with respect to nonideal circuit behavior.

The paper is divided into three main sections. Section II presents the architecture of the oversampling  $\Pi\Delta\Sigma$ ADC. Section III extends the previously presented nonoversampling  $\Pi\Delta\Sigma$ ADC theory to allow for oversampling, considers the performance and complexity of hardware-efficient digital decimation filters and equalizers, presents numerous graphs indicating the quantization error performance as a function of  $M$ ,  $N$ , and  $\Delta\Sigma$  modulator order, and presents expressions for the additional error caused by arbitrary gain and offset deviations introduced by nonideal analog circuitry. Section IV applies the results of the previous section to a detailed analysis of the four-channel system mentioned above.

## II. ARCHITECTURE

The oversampling  $\Pi\Delta\Sigma$ ADC architecture is shown in Fig. 1. The structure is related to that of an  $M$ -path digital filter [11]. On each channel, the analog input sequence  $x[n]$  is modulated by an analog  $\pm 1$  sequence  $v_r[n]$ ,  $\Delta\Sigma$  modulated, decimated filtered, and modulated by a digital  $\pm 1$  sequence  $u_r[n]$ . The outputs of the  $M$  channels are summed to produce the  $\Pi\Delta\Sigma$ ADC output  $y[n]$ . The part of the  $\Pi\Delta\Sigma$ ADC that contains the analog modulators and the  $\Delta\Sigma$  modulator is referred to as the  $\Pi\Delta\Sigma$  modulator. The part of the  $\Pi\Delta\Sigma$ ADC that includes the decimation filters, digital modulators, and the channel summers is referred to as the decoder.

The  $\Delta\Sigma$  modulators, in principle, can be of any type. Independent of the type, the output of a  $\Delta\Sigma$  modulator can be viewed as the sum of a *signal component* and a *quantization error component*. To simplify the analyses that follow, it is assumed that the  $\Delta\Sigma$  modulators are such that the signal component is just an  $L$ -sample delayed version of the  $\Delta\Sigma$  modulator input sequence and that the quantization error component is well modeled as the output of a filter

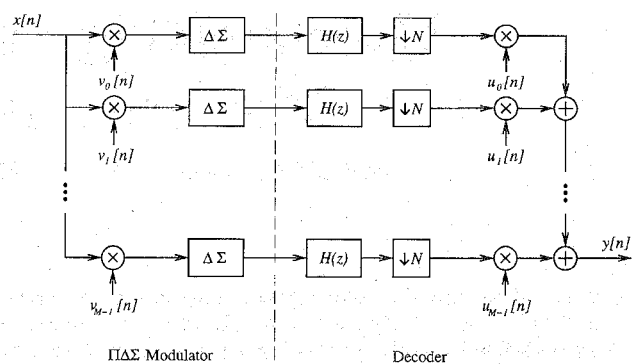


Fig. 1. The oversampling  $\Pi\Delta\Sigma$  A/D converter architecture.

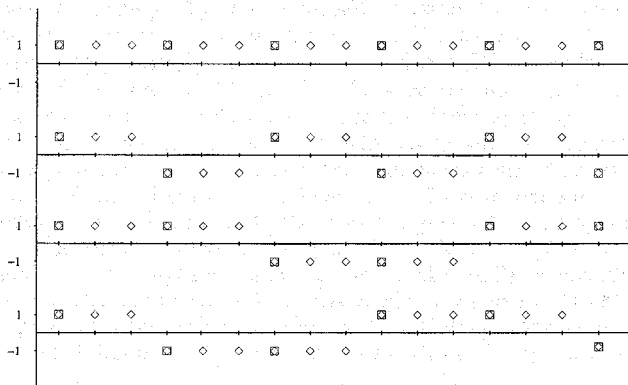


Fig. 2. Example Hadamard modulation sequences for the  $\Pi\Delta\Sigma$ ADC with  $M = 4$ ,  $N = 3$ , and  $k_0 = 3$ . The diamonds correspond to  $v_r[n]$  and the squares correspond to  $u_r[n]$ . The graphs are plotted against time; the tick marks represent sample-times of the input sequence. Each graph corresponds to one channel.

$N(z) = (1 - z^{-1})^P$  driven by white noise. Thus,  $N(z)$  is referred to as the  $\Delta\Sigma$  modulator *noise filter*,  $P$  is referred to as the order of the  $\Delta\Sigma$  modulator, and  $S(z) = z^{-L}$  is referred to as the  $\Delta\Sigma$  modulator *signal filter*. Most of the multiloop  $\Delta\Sigma$  modulator architectures as well as the multistage  $\Delta\Sigma$  modulator architectures fit this paradigm [1], [12]. Notably, interpolative  $\Delta\Sigma$  modulator architectures do not fit this paradigm, but the results of this paper can be modified without introducing new ideas to accommodate such  $\Delta\Sigma$  modulators.

The decimation filters are identical and perform the function of a low-pass filter  $H(z)$  followed by an  $N$ -fold downsampler. The purpose of the low-pass filters is to remove as much as possible of the quantization error component of the  $\Delta\Sigma$  modulators subject to certain restrictions, as detailed in the next section. The next section also presents FIR low-pass filters that are efficient in filtering the quantization error component and have low hardware complexity.

The modulation sequences  $u_r[n]$  and  $v_r[n]$  are derived from an  $M \times M$  Hadamard matrix  $\mathbf{A}$  [13]. Accordingly, they are referred to as *Hadamard sequences*, and the process of multiplying by these sequences is referred to as *Hadamard modulation*. A Hadamard matrix consists exclusively of plus and minus ones and has the property that  $\mathbf{A}^T \mathbf{A} = M \mathbf{I}$ , where  $\mathbf{I}$  is the identity matrix. With  $a(j, k)$  defined as the element in the  $j$ th row and  $k$ th column of  $\mathbf{A}$ ,  $0 \leq j, k \leq M - 1$ , the

Hadamard sequences are

$$u_r[n] = a(r, n \bmod M)$$

and

$$v_r[n] = u_r\left(\left\lfloor \frac{n + k_0}{N} \right\rfloor\right)$$

where  $k_0 = \frac{J+N}{2} - 1 + L$  and  $J$  is the length of  $H(z)$ . Fig. 2 shows an example of the Hadamard sequences for  $M = 4$ ,  $N = 3$ , and  $k_0 = 3$ . Hadamard modulation is thus a simple process; for the sequence  $v_r[n]$  it requires the capability of analog sign inversion, and for the sequence  $u_r[n]$  it requires the capability of digital sign inversion.

### III. THEORETICAL PERFORMANCE

In this section, the performance of the oversampling  $\Pi\Delta\Sigma$ ADC is analyzed in detail. Because the nonoversampling  $\Pi\Delta\Sigma$ ADC has been presented in [9], the presentation in this section refers to the results in [9] whenever possible. For instance, a simple example that explains the heuristics of the  $\Pi\Delta\Sigma$ ADC idea is presented in [9], so no similar example is presented here. Similarly, some of the results in this section are straightforward extensions of corresponding results in [9], so they are simply stated without derivation. However, several of the results are unique to the oversampling  $\Pi\Delta\Sigma$ ADC, and are derived fully.

#### A. The Overall Signal and Quantization Error Components

As with the nonoversampling  $\Pi\Delta\Sigma$ ADC, the output of the oversampling  $\Pi\Delta\Sigma$ ADC can be viewed as the sum of an overall signal component and an overall quantization error component, i.e.,

$$y[n] = w[n] + e_q[n]$$

where  $w[n]$  denotes the overall signal component and  $e_q[n]$  denotes the overall quantization error component. Using an analysis similar to that presented in [9], it can be shown that  $w[n]$  is a linear time-invariant (LTI) filtered and  $N$ -fold downsampled version of the input sequence. In the following,  $H'(z)$  denotes the LTI filter to which  $x[n]$  is subjected before downsampling, i.e., the transfer function from  $x[n]$  to  $w[n]$  ignoring downsampling. For the special case where  $H(z)$  is a length- $J$  FIR filter, a straightforward extension of the analysis in [9] leads to

$$H'(z) = Mz^{-L} \sum_{i=-T}^T \sum_{k=iMN+\frac{J-N}{2}}^{iMN+\frac{J+N}{2}-1} h[k]z^{-k} \quad (1)$$

where  $J$  and  $N$  must either both be even or both be odd integers. The summing limit  $T$  equals  $\lceil \frac{J-1}{2MN} \rceil$  if  $J$  and  $N$  are odd, and  $T$  equals  $\lceil \frac{J-1}{MN} \rceil$  if  $J$  and  $N$  are even.

The distortion of  $w[n]$  resulting from the roll-off of  $H'(e^{j\omega})$  can be compensated with an equalization filter placed after the  $\Pi\Delta\Sigma$ ADC. As will be shown, a practical equalization filter can be obtained provided  $H'(e^{j\omega})$  does not have zeros within

the interval  $(-\frac{\pi}{N}, \frac{\pi}{N})$ . In this case, the ideal equalization filter has frequency response

$$F(e^{j\omega}) = \frac{1}{H'(e^{j\frac{\omega}{N}})}, \quad |\omega| \leq \pi \quad (2)$$

which, in general, is a noncausal IIR filter with a nonlinear phase response. A practical equalization filter must have a frequency response that closely approximates (2) aside from a delay factor. An example of such a filter is presented in Section IV.

An important property that is unique to  $\Pi\Delta\Sigma$ ADC's relative to conventional  $\Delta\Sigma$ ADC's follows from (1). For both  $\Pi\Delta\Sigma$ ADC's and conventional  $\Delta\Sigma$ ADC's, the purpose of the low-pass filtering is to attenuate the quantization error as much as possible without distorting the signal component beyond repair. For conventional  $\Delta\Sigma$ ADC's, the low-pass filter must not have zeros within the interval  $(-\frac{\pi}{N}, \frac{\pi}{N})$  because it also filters the input sequence. In the  $\Pi\Delta\Sigma$ ADC architecture, however, different filters are applied to the input sequence and the quantization error components; namely,  $H'(z)$  and  $H(z)$ , respectively. Notice from (1) that  $H'(z)$  is independent of many of the samples of the impulse response of  $H(z)$ . Specifically, the equation indicates that  $H'(z)$  only depends on every length- $N$  band of  $h[n]$  symmetric about every  $MN$ th sample relative to the center sample. Consequently, the low-pass filter can be chosen to have a considerably narrower passband than  $(-\frac{\pi}{N}, \frac{\pi}{N})$ , resulting in more efficient filtering of the quantization error components than in conventional  $\Delta\Sigma$ ADC's, while still allowing for signal recovery. This is demonstrated in the next section.

#### B. The Equalized Overall Quantization Error Component

A meaningful measure of the  $\Pi\Delta\Sigma$ ADC quantization error performance is the power of the overall quantization error component after perfect equalization, which can be written as

$$P_e = \frac{1}{2\pi} \int_{-\pi}^{\pi} S_{ee}(e^{j\omega}) d\omega \quad (3)$$

where  $S_{ee}(e^{j\omega})$  is the power spectral density (PSD) of the overall quantization error component after ideal equalization. Thus,

$$S_{ee}(e^{j\omega}) = S_{e_q e_q}(e^{j\omega}) |F(e^{j\omega})|^2 \quad (4)$$

where  $S_{e_q e_q}(e^{j\omega})$  is the power spectral density of the overall quantization error component. The  $\Pi\Delta\Sigma$ ADC without equalization can be viewed as a perfectly equalized A/D converter with quantization error power  $P_e$  followed by  $H'(z)$ . Therefore,  $P_e$  is a measure of A/D converter performance that is independent of whether or how accurately the equalization filter is implemented (which depends on the application).

To evaluate (3), it is necessary to derive an expression for  $S_{e_q e_q}(e^{j\omega})$ . This has been done in [9] for the special case of  $N = 1$ , and a straightforward generalization of the derivation

leads to

$$S_{e_q e_q}(e^{j\omega}) = \frac{\Delta^2}{12N} \sum_{n=0}^{M-1} \sum_{k=0}^{N-1} \left| N(e^{j(\omega-2\pi(\frac{n}{M}+k))/N}) H(e^{j(\omega-2\pi(\frac{n}{M}+k))/N}) \right|^2 \quad (5)$$

where  $\Delta$  is the quantization step-size of the coarse A/D converters in the  $\Delta\Sigma$  modulators. Substituting (5) into (3) and integrating over the interval  $(-\pi, \pi)$  eventually yields the following simplified expression for the power of the overall quantization error component after equalization

$$P_e = \frac{\Delta^2}{24\pi} \int_{-\pi}^{\pi} \sum_{n=0}^{M-1} \left| N(e^{j(\omega-2\pi\frac{n}{MN})}) H(e^{j(\omega-2\pi\frac{n}{NM})}) F(e^{j\omega N}) \right|^2 d\omega. \quad (6)$$

This expression is used to numerically calculate  $P_e$  in the following subsections.

### C. Comb<sup>P+1</sup> Filtering

As is apparent from (6),  $P_e$  depends on  $H(e^{j\omega})$ , so it is essential to choose channel filters that result in as small a value of  $P_e$  as is practical. The practicality constraint is that the filters also must be simple to implement in hardware. As will now be shown, the use of comb<sup>P+1</sup> filters [14], [15] results in very small values of  $P_e$ . Moreover, hardware-efficient structures with which to implement these filters are well known [14].

A general form of the comb<sup>P+1</sup> filter transfer function is

$$H(z) = \left( \frac{1-z^{-J_1}}{1-z^{-1}} \right)^{P_1} \left( \frac{1-z^{-J_2}}{1-z^{-1}} \right)^{P_2} \quad (7)$$

where  $J_2 = J_1 + 1$  and  $P + 1 = P_1 + P_2$ . The reason for using this two-factor form of the comb<sup>P+1</sup> transfer function is that it does not place any restrictions on the impulse response length; filters of any length  $J$  can be obtained with the appropriate choice of  $P_1$ ,  $P_2$ , and  $J_1$ . In particular, it is easy to verify that  $J = P_1(J_1 - 1) + P_2 J_1 + 1$ .

Fig. 3 shows the dependence of  $P_e$  in dB relative to  $\Delta^2$  on comb<sup>P+1</sup> filter length for the specific case of a four-channel  $\Pi\Delta\Sigma$ ADC with tenfold oversampling and fourth-order  $\Delta\Sigma$  modulators (i.e.,  $M = 4$ ,  $N = 10$ , and  $P = 4$ ). The data were numerically calculated using (6) with  $H(e^{j\omega})$  corresponding to (7). As is evident from the figure,  $P_e$  decreases initially with filter length, eventually reaching a minimum,  $P_{e_{\min}}$ . Thereafter it begins to increase. This behavior of the dependency of  $P_e$  on comb<sup>P+1</sup> filter length  $J$  can be explained as follows. First, recall that  $P_e$  is the power of the quantization error component of the equalized  $\Pi\Delta\Sigma$ ADC output. For small values of  $J$ ,  $H(e^{j\omega})$  is a poor low-pass filter and a relatively large amount of quantization error passes through to  $y[n]$ . In this case, the gain of  $F(e^{j\omega})$  is close to unity, and therefore does not appreciably affect the overall quantization error component. As  $J$  is increased,  $H(e^{j\omega})$  increasingly attenuates the quantization error while the gain of  $F(e^{j\omega})$

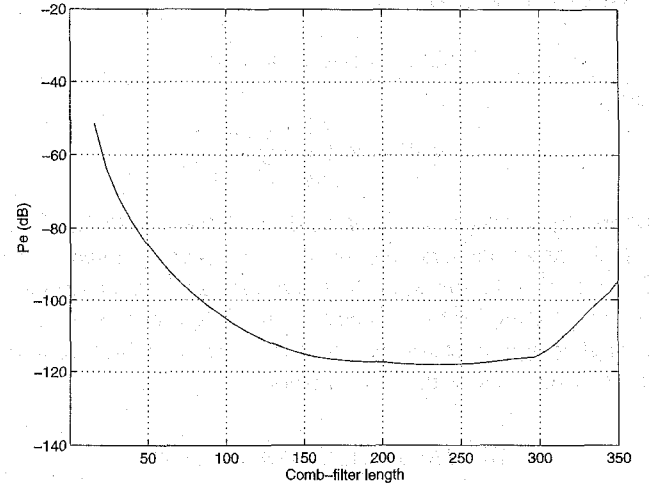


Fig. 3. Dependence of  $P_e$  in dB relative to  $\Delta^2$  on comb<sup>P+1</sup> filter length for the example four-channel  $\Pi\Delta\Sigma$ ADC.

remains moderate. The net result is to decrease  $P_e$ . As  $J$  increases further, signal distortion becomes considerable and no net reduction of  $P_e$  is possible because of the large gain of  $F(e^{j\omega})$ . At this point, the minimum value of  $P_e$  has been reached. Increasing  $J$  further results in a net increase of  $P_e$  caused by the ever increasing gain of  $F(e^{j\omega})$ .

The minimum attainable  $P_e$  for this example is  $-118$  dB relative to  $\Delta^2$  when employing the length-248 comb<sup>5</sup> filter with transfer function given by (7) for  $P_1 = 3$ ,  $P_2 = 2$ ,  $J_1 = 50$ , and  $J_2 = 51$ . As a comparison, the power of the quantization error introduced by a conventional  $\Delta\Sigma$ ADC with a fortyfold oversampling, fourth-order  $\Delta\Sigma$  modulator is approximately  $-124$  dB relative to  $\Delta^2$ , as can be verified from the analysis presented in [1].

Fig. 4 shows  $P_{e_{\min}}$  as a function of  $M$  and  $N$  on log base-two scales for  $\Delta\Sigma$  modulators of orders two through six. Each plot corresponds to different  $\Delta\Sigma$  modulator orders. Each plotted line corresponds to the loci of equal values of  $P_{e_{\min}}$  as a function of  $\log_2 M$  and  $\log_2 N$ . As can be inferred from the data, for every doubling of the oversampling ratio,  $P_{e_{\min}}$  decreases by  $(6P + 3)$  dB which corresponds to  $(P + \frac{1}{2})$  additional bits of conversion precision [16], independent of the number of channels in the architecture. This result is analogous to the performance increase of  $\Delta\Sigma$ ADC's when doubling the oversampling ratio. As can also be inferred from the figures, for every doubling of the number of channels,  $P_{e_{\min}}$  decreases by  $6P$  dB, corresponding to  $P$  additional bits of conversion precision, independent of oversampling ratio. Thus, aside from a 3 dB difference, the performance increase resulting from doubling  $M$  is equivalent to the performance increase resulting from doubling  $N$ . This difference of 3 dB is related to the doubling of the power of the overall quantization error component that results when the number of uncorrelated quantization error components added in the decoder is doubled, as further described in [9].

The above findings result in the conclusion that an  $N$ -fold oversampling,  $M$ -channel  $\Pi\Delta\Sigma$ ADC performs equivalently to an  $M \times N$ -fold oversampling  $\Delta\Sigma$ ADC, aside from a  $\frac{1}{2} \log_2(M)$ -b penalty associated with the parallel structure.

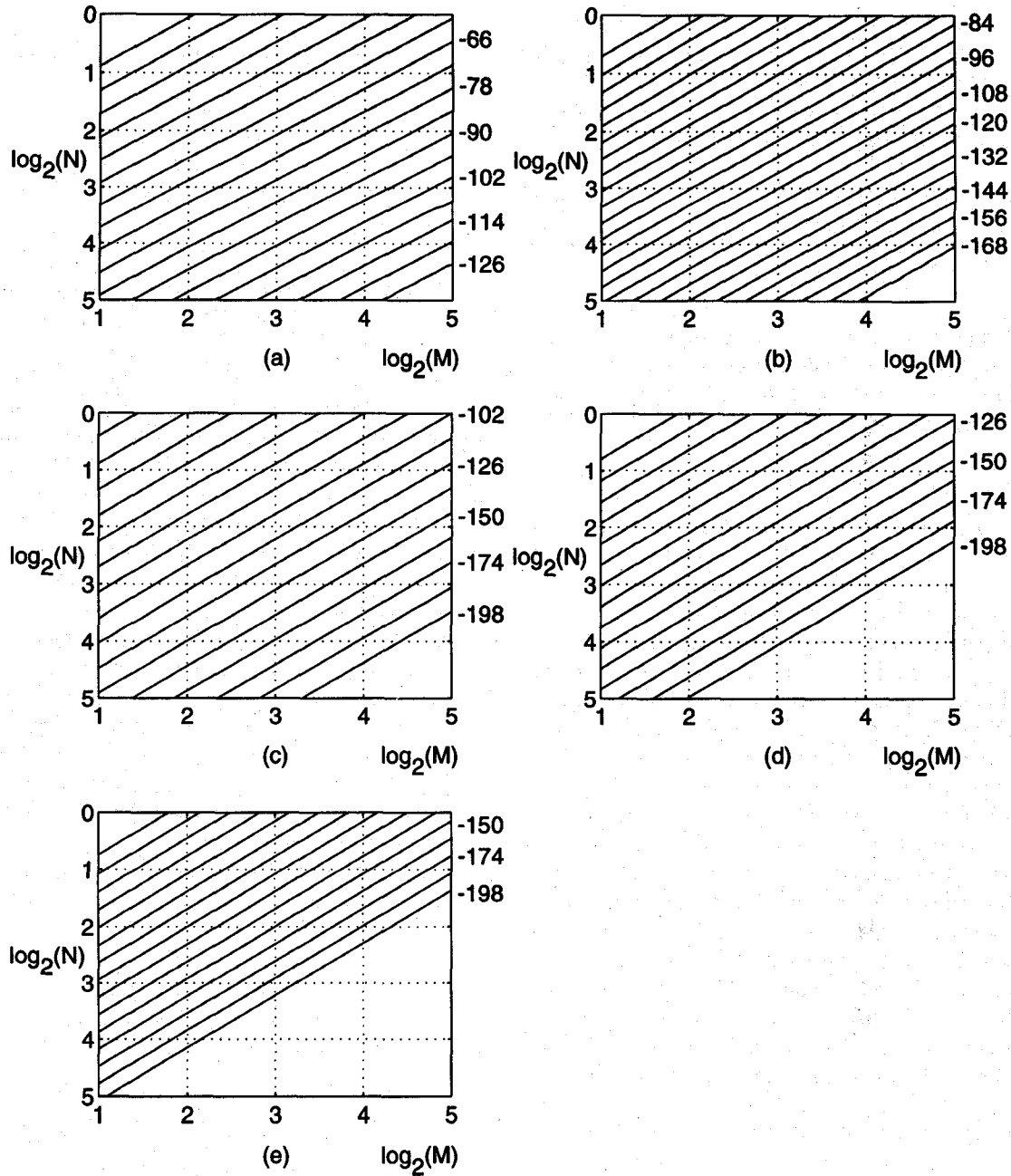


Fig. 4. Minimum attainable  $P_e$  in dB relative to  $\Delta^2$  when using  $\text{comb}^{P+1}$  low-pass filters versus  $M$  and  $N$  on log base-two scales of the  $\Pi\Delta\Sigma$  ADC with (a) second-order, (b) third-order, (c) fourth-order, (d) fifth-order, and (e) sixth-order  $\Delta\Sigma$  modulators.

Although the filters used to generate the data of Fig. 4 were of the general form (7), typically a performance equal or close to  $P_{e_{\min}}$  can be obtained using a  $\text{comb}^{P+1}$  filter with the simpler transfer function

$$H(z) = \left( \frac{1 - z^{-kN}}{1 - z^{-1}} \right)^{P+1} \quad (8)$$

where  $k$  is a small positive integer. This property holds because the dependence of  $P_e$  on  $\text{comb}^{P+1}$  filter length exhibits a "flat region" in which  $P_e$  is approximately constant and equal to  $P_{e_{\min}}$ , allowing for the use of a filter of the form (8) that happens to lie within this region. For the example four-channel  $\Pi\Delta\Sigma$  ADC, it is evident from Fig. 3 that the "flat region"

occurs for the filters with lengths between 180 and 300. In particular, a  $P_e$  of  $-117$  dB relative to  $\Delta^2$  is obtainable with the length-196 filter

$$H(z) = \left( \frac{1 - z^{-4 \times 10}}{1 - z^{-1}} \right)^5 \quad (9)$$

i.e., a filter of the form (8) where  $k = 4$ .

#### D. Equalizing the $\Pi\Delta\Sigma$ ADC Output

For applications in which the roll-off associated with  $H'(z)$  is not a problem or in which equalization can be incorporated into subsequent signal processing stages, it may not be necessary to actually implement the equalization filter. For

other applications, where signal equalization must be part of the ADC, an equalization filter may be cascaded with the  $\Pi\Delta\Sigma$ ADC. Although the ideal equalization filter  $F'(e^{j\omega})$  of (2) is a noncausal IIR filter, a delayed version of it can be well-approximated using a causal FIR equalization filter  $F'(e^{j\omega})$ .

Applying the Parks-McClellan algorithm [17],  $F'(e^{j\omega})$  can be designed optimally in the sense that the overall signal filter

$$H'(e^{j\frac{\omega}{N}})F'(e^{j\omega}) \quad (10)$$

is equiripple and linear phase. As demonstrated in the next section, the ripple decreases with increasing filter length, and equalization filters  $F'(e^{j\omega})$  that result in arbitrarily small peak ripple can be designed.

### E. Sensitivity to Nonideal Circuit Behavior

In practice, nonideal circuit behavior reduces the conversion precision below that predicted by the theoretical analysis presented above. As discussed in [9], it is convenient to distinguish between two types of errors caused by nonideal circuit behavior: those that are common to conventional  $\Delta\Sigma$ ADC's, and those that are unique to the  $\Pi\Delta\Sigma$ ADC. This allows existing results concerning nonideal circuit behavior in conventional  $\Delta\Sigma$ ADC's to be applied directly to  $\Pi\Delta\Sigma$ ADC's. Specifically, the error arising from nonideal circuit behavior can be considered the sum of two subcomponents: the *conversion error subcomponent*, denoted as  $e_{\Delta\Sigma}[n]$ , and the *reconstruction error subcomponent*, denoted as  $e_{\Pi}[n]$ . The conversion error subcomponent is the result of all types of nonideal  $\Delta\Sigma$  modulator performance except for  $\Delta\Sigma$  modulator signal component gain and offset errors. The reconstruction error subcomponent is the aggregate of all A/D conversion errors arising from nonideal circuit behavior that are not part of the conversion error subcomponent such as channel gain and offset errors, Hadamard level errors, etc. With these definitions, the  $\Pi\Delta\Sigma$ ADC output can be written as

$$y[n] = w[n] + e_q[n] + e_{\Delta\Sigma}[n] + e_{\Pi}[n].$$

Each channel of a  $\Pi\Delta\Sigma$ ADC contains the equivalent of a conventional  $\Delta\Sigma$ ADC with a low-pass filter appropriate for an oversampling ratio of close to  $M \times N$ . Thus, the component of the sequence just prior to Hadamard modulation in the decoder arising from nonideal  $\Delta\Sigma$  modulator behavior has approximately the same power as the corresponding component of the output of a conventional  $\Delta\Sigma$ ADC with oversampling ratio  $M \times N$ . In general, the  $M$  such error components are correlated. However, they originate from sources located after the analog Hadamard modulators in the  $\Pi\Delta\Sigma$  modulator, so they are decorrelated by the subsequent digital Hadamard modulators. As a result, they add in power, not amplitude; the power of the conversion error subcomponent is simply the sum of the powers of the low-pass filtered errors from the  $M$  nonideal  $\Delta\Sigma$  modulators. It follows that the power of  $e_{\Delta\Sigma}[n]$  is approximately equal to the power of the error arising from nonideal circuit behavior at the output of a conventional  $\Delta\Sigma$ ADC with oversampling ratio  $N$ .

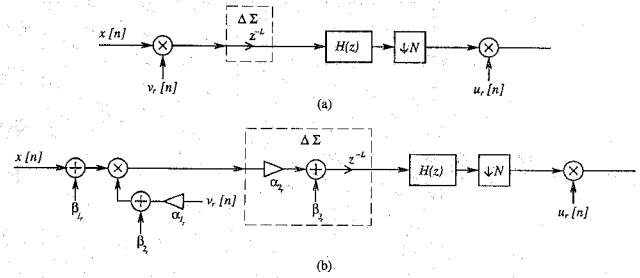


Fig. 5. Signal equivalent circuits of the  $r$ th channel for (a) ideal circuit behavior and (b) nonideal circuit behavior.

Unlike the conversion error subcomponent, the reconstruction error subcomponent  $e_{\Pi}[n]$  does not have a direct analogy in conventional  $\Delta\Sigma$ ADC's. It results from nonideal analog Hadamard modulator behavior and from mismatches among the signal component gains and offsets of the  $\Delta\Sigma$  modulators. Fig. 5(a) shows the ideal processing performed on the input sequence by each channel neglecting quantization error and Fig. 5(b) shows the same thing except with all possible error sources that contribute to  $e_{\Pi}[n]$ . As shown,  $\beta_{1r}$  represents an offset prior to analog Hadamard modulation,  $\alpha_{1r}$  and  $\beta_{2r}$  represent the amplitude and offset, respectively, of the Hadamard sequence, and  $\alpha_{2r}$  and  $\beta_{3r}$  represent the gain and offset, respectively, of the  $\Delta\Sigma$  modulator. In the general case,  $\alpha_{1r}$ ,  $\alpha_{2r}$ ,  $\beta_{1r}$ ,  $\beta_{2r}$ , and  $\beta_{3r}$  could all be time-varying functions. It follows that all circuit errors specific to the  $\Pi\Delta\Sigma$ ADC can be included in the equivalent circuit of Fig. 5(b). Together, these circuit errors give rise to  $e_{\Pi}[n]$ .

From Fig. 5(a), it follows that the ideal signal component of the output of the  $r$ th  $\Delta\Sigma$  modulator is

$$x[n-L]v_r[n-L].$$

However, Fig. 5(b) indicates that with nonideal circuit behavior corresponding to  $e_{\Pi}[n]$ , the signal component of the output of the  $\Delta\Sigma$  modulator is

$$(1 + a_r)x[n-L]v_r[n-L] + b_r x[n-L] + c_r v_r[n-L] + d_r,$$

where  $a_r = \alpha_{1r}\alpha_{2r} - 1$ ,  $b_r = \alpha_{2r}\beta_{2r}$ ,  $c_r = \alpha_{1r}\alpha_{2r}\beta_{1r}$ , and  $d_r = \alpha_{2r}\beta_{1r}\beta_{2r} + \beta_{3r}$ .

A straightforward extension of the analysis presented in [9] leads to the following expression for the reconstruction error subcomponent

$$\begin{aligned} e_{\Pi}[n] = & \sum_{r=0}^M a_r v_r[nN-k] u_r[n] \sum_{k=-\infty}^{\infty} h'[k] x[nN-k] \\ & + \sum_{r=0}^M b_r u_r[n] \sum_{k=-\infty}^{\infty} h'[k] x[nN-k] \\ & + \sum_{r=0}^M c_r v_r[nN-k] u_r[n] \sum_{k=-\infty}^{\infty} h'[k] \\ & + \sum_{r=0}^M d_r u_r[n] \sum_{k=-\infty}^{\infty} h'[k]. \end{aligned} \quad (11)$$

Thus,  $e_{\Pi}[n]$  is linear in each of  $a_r$ ,  $b_r$ ,  $c_r$ , and  $d_r$ , from which it follows that the effect of each term on  $e_{\Pi}[n]$  can

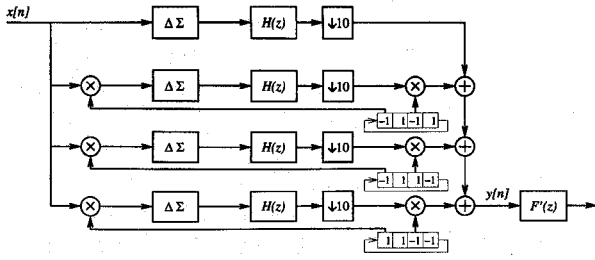


Fig. 6. The example  $\Pi\Delta\Sigma$ ADC architecture with an equalization filter following the output.

be considered separately and summed to obtain the net effect. This is demonstrated for the design example presented in the next section.

From (11) it is evident that the terms associated with  $c_r$  and  $d_r$  do not depend upon  $x[n]$ . Indeed, in the case of the design example presented in the next section, the term associated with  $c_r$  reduces to a dc offset, and the term associated with  $d_r$  reduces to the sum of a dc offset, a half-rate sinusoid, and a full-rate sinusoid.

#### IV. A DESIGN EXAMPLE

##### A. The Example $\Pi\Delta\Sigma$ ADC Parameters

The example  $\Pi\Delta\Sigma$ ADC to be considered in detail in this section is shown followed by an equalization filter in Fig. 6. It is a four-channel system with tenfold oversampling and fourth-order  $\Delta\Sigma$  modulators (i.e.,  $M = 4$ ,  $N = 10$ , and  $P = 4$ ). In all the calculations and simulations performed in this and the next section, the  $\Delta\Sigma$  modulators are taken to each consist of two cascaded second-order double-loop  $\Delta\Sigma$  modulators [1], [5] each with three-level A/D and D/A converters [6]. The low-pass filters have the transfer function given by (9).

Because of the tenfold oversampling, there are two system clock frequencies. These will be referred to as the *input sample-rate*  $f_i$  and the *output sample-rate*  $f_o$ , respectively. In this example, it follows that  $f_i = 10 \cdot f_o$ . (for example, reasonable values might be  $f_i = 20$  MHz and  $f_o = 2$  MHz). All of the circuitry corresponding to the portion of Fig. 6 to the left of the tenfold downsamplers is clocked at the input sample-rate and all that to the right of the tenfold downsamplers is clocked at the output sample-rate.

The Hadamard sequences are generated by the three length-4,  $f_o$ -rate shift registers. Only three shift registers are necessary because the Hadamard sequence for the top channel in Fig. 6 is the all-ones sequence. The timing is such that each analog Hadamard modulator multiplies 10 samples of  $x[n]$  by one shift register sample during the same time that each digital Hadamard modulator multiplies one decimation filter output sample by one shift register sample.

The magnitude responses associated with  $H(z)$  and  $H'(z)$  are shown in Fig. 7(a) as solid and dashed curves, respectively. The characteristic property of the  $\Pi\Delta\Sigma$ ADC that the passband of  $H(z)$  can be made considerably narrower than that of  $H'(z)$  is evident from the figure. In this case, the lowest frequency zeros of  $H(e^{j\omega})$  and  $H'(e^{j\omega})$  occur for  $\omega = \pm \frac{\pi}{20}$  radians and  $\omega = \pm \frac{\pi}{5}$  radians, respectively.

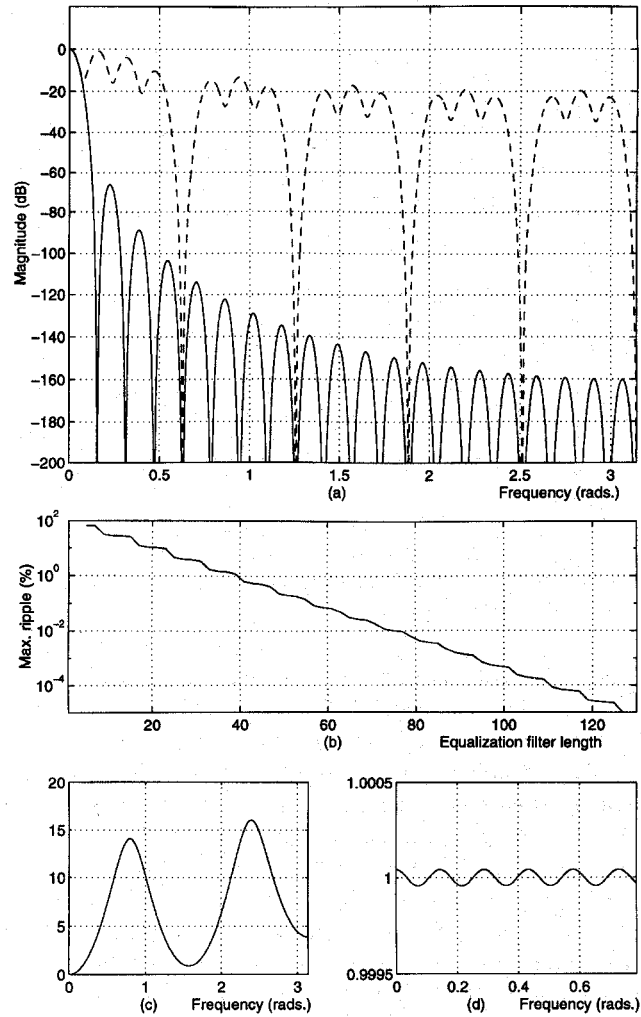


Fig. 7. (a) Magnitude response in dB of the low-pass filter  $H(e^{j\omega})$  (solid line) and the signal filter  $H'(e^{j\omega})$  (dashed line). (b) Maximum ripple in percentage of the ideal  $\Pi\Delta\Sigma$ ADC overall signal filter passband amplitude versus equalization filter length. (c) Magnitude response in dB of the length-81 equalization filter. (d) Equiripple magnitude response of the overall signal filter shown for the frequency range  $(0, \frac{\pi}{4})$  radians.

The dependence of the peak passband ripple of the overall signal filter on the length of the optimal equalization filter is shown in Fig. 7(b). The datum for each filter length was obtained by generating an optimal equalization filter of the desired length, as outlined in the previous section, and then finding its maximum ripple value. As an example, the magnitude response of a length-81 optimal equalization filter is shown in Fig. 7(c), and Fig. 7(d) shows a magnified view of a portion of the passband magnitude of the corresponding overall signal filter. As expected, the overall signal filter magnitude response is equiripple. Its peak ripple is 0.004% of the ideal passband value, corresponding to 0.0003 dB.

##### B. The Ideal A/D Conversion Performance

Fig. 8 shows both calculated and simulated data for the example  $\Pi\Delta\Sigma$ ADC. Fig. 8(a) shows the theoretical PSD of the overall quantization error component after equalization,  $S_{ee}(e^{j\omega})$ , calculated using the results of the previous section. Fig. 8(b) shows the estimated PSD of the equalized output

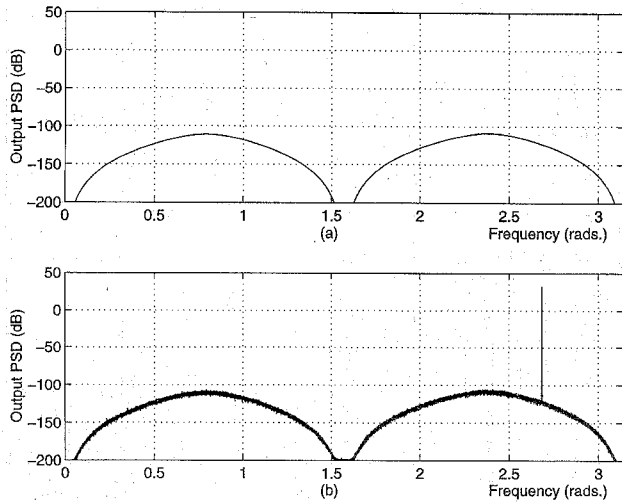


Fig. 8. (a) Calculated PSD in dB relative to  $\Delta^2$  of the equalized  $e_q[n]$  of the example  $\Pi\Delta\Sigma$ ADC as found by evaluating (5). (b) PSD of the equalized simulated output the example  $\Pi\Delta\Sigma$ ADC corresponding to a sinusoidal input and ideal circuit behavior.

of the  $\Pi\Delta\Sigma$ ADC as obtained by computer simulation for a sinusoidal input sequence of amplitude  $0.40\Delta$  and frequency  $\frac{875}{1024}\pi$  radians. The spectral estimation was performed by averaging 15 periodograms corresponding to half-overlapping Hanning windowed length- $2^{16}$  segments of the simulated  $\Pi\Delta\Sigma$ ADC output, and scaling the result by  $|F(e^{j\omega})|^2$  to achieve equalization. Because the input sequence was a sinusoid, it is easy to visually separate the equalized overall signal component—the large spur—from the equalized overall quantization error component—everything else—in the data shown in Fig. 8(b). With this in mind, it is evident from Fig. 8 that the theoretically calculated PSD matches the PSD obtained by simulation extremely well. For instance, numerically integrating the two sets of PSD data to obtain values of  $P_e$  corresponding to theory and simulation yield  $-118$  and  $-117$  dB, respectively, relative to  $\Delta^2$ .

Simulations indicate that a conservative estimate of the usable input range of the fourth-order  $\Delta\Sigma$  modulators with 3-level quantizers is  $(-0.4\Delta, 0.4\Delta)$ . Therefore, the obtained value of  $P_e$  corresponds to an A/D conversion precision of 18 b [15].

### C. Digital Hardware Complexity

The example  $\Pi\Delta\Sigma$ ADC decoder employs 4 comb<sup>5</sup> filters and 3 adders to sum the channels. A hardware efficient structure that implements the functionality of the comb<sup>5</sup> filter with transfer function given by (9) followed by a tenfold downsampler is shown in Fig. 9 [14]. Evidently, each filter requires 5  $f_i$ -rate adders and 5  $f_o$ -rate adders. Referring the rate of additions to  $f_i$  (i.e., one unit of time is considered to be  $1/f_i$ ), this corresponds to 5.5 additions per unit time (APU's). Furthermore, 20 delay elements are required. Considering all 4 channels, the decoder requires a total of 22.3 APU's and 80 delay elements. The example equalization filter is of length 81 with symmetric coefficients. Therefore, the implementation requires 8 APU's, 4 multiplications per unit time (MPU's), and 80 delay elements.

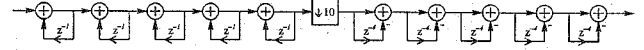


Fig. 9. A commonly used hardware efficient structure that performs the function of the comb<sup>5</sup> transfer function given by (9) followed by tenfold downsampling in the example  $\Pi\Delta\Sigma$ ADC.

It follows that the total requirement for the decoder and equalization filter is 30.3 APU's, 4 MPU's, and 160 delay elements. By comparison, the corresponding digital hardware complexity for a conventional fourth-order  $\Delta\Sigma$ ADC [5] is 58.42 APU's and 12.3 MPU's where, to facilitate comparison, a unit of time has been taken to be one-tenth of the reciprocal of the A/D conversion rate.

It follows, in this case, that the digital complexity of the  $\Pi\Delta\Sigma$ ADC actually is lower than that of the corresponding  $\Delta\Sigma$ ADC. In the general case, all  $M$  of the channel filters in a  $\Pi\Delta\Sigma$ ADC together tend to require approximately the same amount of digital processing as the first stage of the decimation filter typically used in a conventional  $\Delta\Sigma$ ADC with comparable A/D conversion performance. This occurs because even though the  $\Pi\Delta\Sigma$ ADC requires  $M$  times as many filters as the conventional  $\Delta\Sigma$ ADC they run at approximately an  $M$ th of the rate of the first-stage filter in the conventional  $\Delta\Sigma$ ADC.

### D. Nonideal Circuit Behavior

Recall from the previous section that only the two terms of (11) corresponding to  $a_r$  and  $b_r$  depend on the input sequence. It can be verified from (11) that for this example system, the error term corresponding to  $c_r$  reduces to a dc offset, and the error term corresponding to  $d_r$  reduces to the sum of a dc offset, a sinusoid of frequency  $f_o/2$  (i.e., a scaled version of the sequence  $\dots, 1, -1, 1, -1, \dots$ ), and a sinusoid of frequency  $f_o/4$  (i.e., a linear combination of the sequence  $\dots, 0, 1, 0, -1, 0, \dots$  and its one-sample shifted counterpart).

Figs. 10 and 11 present simulation data that demonstrate the effect of the four terms of (11) on the spurious-free dynamic range of the equalized example  $\Pi\Delta\Sigma$ ADC output and the power of  $e_q[n] + e_{\Pi}[n]$ , respectively. Recall from the previous section that each of these four terms are affected only by the set of  $M$  values corresponding to one of  $a_r, b_r, c_r$ , or  $d_r$ . Thus, for each plot in both figures, only one set of these values was nonzero, thereby isolating the effect of each of the four terms in (11). The data were generated by simulating  $\Pi\Delta\Sigma$ ADC's wherein these nonzero values were chosen randomly within the ranges of  $\pm 10^{-6}\Delta, \pm 10^{-5}\Delta, \pm 10^{-4}\Delta, \pm 10^{-3}\Delta$ , and  $\pm 10^{-2}\Delta$ . Each point type +, \*, o, or x, corresponds to a different  $\Pi\Delta\Sigma$ ADC simulation in which the random values were chosen with a different random number seed. The solid lines represent averages of the plotted data.

The data of Figs. 10 and 11 indicate that the error is not highly sensitive to the values of  $a_r$  and  $b_r$  and is independent of the values of  $c_r$  (which makes sense because the error term corresponding to  $c_r$  is simply a dc offset). For example, the data indicate that provided the values of  $a_r$  and  $b_r$  are within about  $\pm 10^{-2}\Delta$  then the corresponding spurious-free



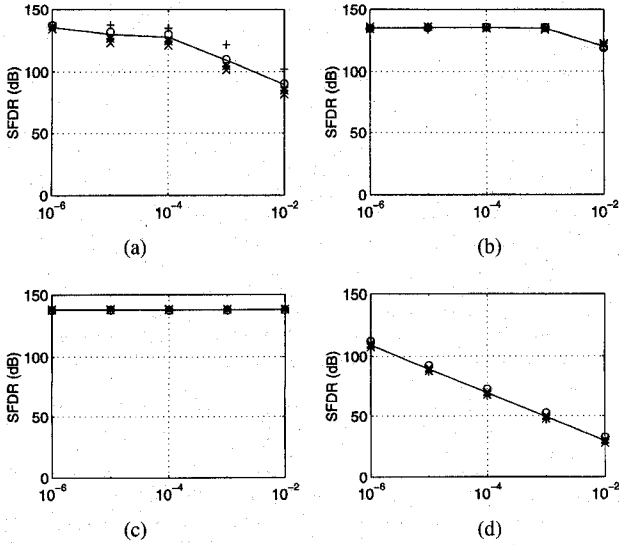


Fig. 10. Spurious-free dynamic range in dB of the equalized example  $\Pi\Delta\Sigma$ ADC output versus the standard deviation of (a)  $a_r/\Delta$ , (b)  $b_r/\Delta$ , (c)  $c_r/\Delta$  and (d)  $d_r/\Delta$ , respectively.

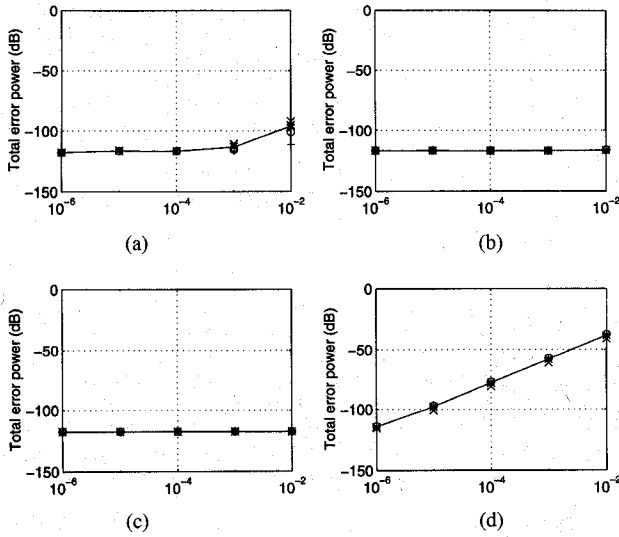


Fig. 11. Power in dB relative to  $\Delta^2$  of the sum of  $e_q[n]$  and  $e_r[n]$  of the equalized output of the example  $\Pi\Delta\Sigma$ ADC versus the standard deviation of (a)  $a_r/\Delta$ , (b)  $b_r/\Delta$ , (c)  $c_r/\Delta$ , and (d)  $d_r/\Delta$ , respectively.

dynamic range is greater than 100 dB and the noise power is below  $-100$  dB relative to  $\Delta^2$ . The resulting A/D conversion performance for the example system is about 16-b. This requires about  $\pm 0.1\%$  gain matching and analog Hadamard level matching.

Unfortunately, the error is quite sensitive to the values of  $d_r$ . For example, to maintain the 16-b level of performance mentioned above, the values of  $d_r$  must be within about  $\pm 5 \cdot 10^{-6}\Delta$ . This corresponds to  $\Delta\Sigma$  modulator offsets that are less than about  $5 \cdot 10^{-6}\Delta$ . However, in most cases it should not be necessary to actually achieve such small offsets for the following two reasons. First, many applications may not be sensitive to the error introduced by the  $d_r$  error term because it is independent of the input sequence and consists of only a dc term and two simple sinusoid terms. For example, a digital notch filter subsequent to the A/D converter can be

used to remove this error at the expense of a partial loss of useable bandwidth. Second, if necessary, the amplitude and phase of the two tones can easily be digitally measured during an autocalibration phase of operation and the tones can be digitally subtracted from the  $\Pi\Delta\Sigma$ ADC output during the normal phase of operation. For example, an autocalibration phase starting at time  $n = 0$  can be performed by setting the input sequence to zero and calculating the values  $A$ ,  $B_I$ , and  $B_Q$  defined as

$$A = \frac{1}{4} \sum_{k=21}^{24} (-1)^k y[k],$$

$$B_I = \frac{1}{2} \sum_{k=21}^{24} \cos(\pi k/2) y[k]$$

and

$$B_Q = \frac{1}{2} \sum_{k=21}^{24} \sin(\pi k/2) y[k].$$

Then, the digitally corrected output during the normal phase of operation is

$$y_c[n] = y[n] - A(-1)^n - B_I \cos(\pi n/2) - B_Q \sin(\pi n/2).$$

Both the  $\cos(\pi k/2)$  and  $\sin(\pi k/2)$  sequences consist of only the values  $\{-1, 0, 1\}$ , so the digital complexity of this scheme is very low. Only four samples of each of the sequences  $(-1)^k y[k]$ ,  $\cos(\pi k/2) y[k]$ , and  $\sin(\pi k/2) y[k]$  are necessary because, as easily can be verified, they are all periodic with period-4 and the goal is to measure their dc components. The whole autocalibration phase requires  $24 f_o$ -rate clock periods. The first 20 periods are necessary for the channel filters to settle (recall that the channel filters have length-196 and the oversampling ratio is 10), and the remaining 4 periods are necessary to perform the measurement. As demonstrated below, the accuracy of the system after autocalibration is essentially as high as would have been achieved had the values of  $d_r$  been zero.

Fig. 12 shows the estimated PSD's of the simulated equalized output of the example  $\Pi\Delta\Sigma$ ADC with nonideal circuit behavior. The parameters for the spectral estimation were the same as for Fig. 9(b). For Fig. 12(a), the circuit errors were chosen so as to obtain random values of  $a_r$  and  $b_r$  to within  $\pm 10^{-2}\Delta$  with  $c_r = d_r = 0$ . For Fig. 12(b),  $a_r$ ,  $b_r$ , and  $d_r$  were chosen randomly to within  $\pm 10^{-2}\Delta$  with  $c_r = 0$  (recall that the term corresponding to  $c_r$  is simply a dc offset). A comparison of the figures reveals that the term of  $e_{\Pi}[n]$  involving  $d_r$  consists of a dc offset plus sinusoids of frequencies  $f_o/4$  and  $f_o/2$ , as expected. Fig. 12(c) shows simulation data with the parameters used to obtain the data in Fig. 12(b) except that the autocalibration scheme and subsequent digital correction described above was employed. As expected, the corrected system performs as well as the system with  $d_r = 0$  for  $0 \leq r \leq 3$ , except for the dc offset.

## V. CONCLUSION

The  $\Pi\Delta\Sigma$ ADC architecture, originally presented as a Nyquist rate A/D converter architecture, has been extended

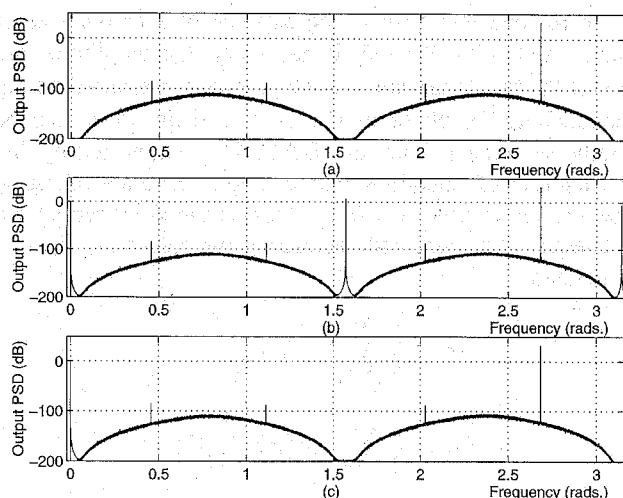


Fig. 12. (a) PSD of the equalized simulated output of the example  $\Pi\Delta\Sigma$  ADC with a sinusoidal input and nonideal circuit behavior corresponding to randomly chosen values of  $a_r$  and  $b_r$  to within  $\pm 10^{-2}\Delta$  while  $c_r = d_r = 0$ . (b) Same as (a) except  $d_r$  randomly chosen to within  $\pm 10^{-2}\Delta$ . (c) Same as (b) except with autocalibration and subsequent digital correction.

to allow for time-oversampling in return for increased precision and reduced analog processing. Through extensions of the theory developed previously for the nonoversampling  $\Pi\Delta\Sigma$  ADC and through computer simulations, it has been shown that an  $M$ -channel system with  $N$ -fold oversampling has performance close to that of a conventional  $\Delta\Sigma$  ADC with  $M \times N$ -fold oversampling. The hardware complexity of the digital filtering circuitry of the  $\Pi\Delta\Sigma$  ADC has been shown to be comparable to that of the corresponding conventional  $\Delta\Sigma$  ADC. The error suffered by the  $\Pi\Delta\Sigma$  ADC as a result of nonideal circuit behavior has been characterized as the sum of two components: a component of the type suffered by conventional  $\Delta\Sigma$  ADC's and a component that is unique to the  $\Pi\Delta\Sigma$  ADC. An explicit expression for the latter component has been presented and supported by simulation data. A four-channel  $\Pi\Delta\Sigma$  ADC with fourth-order  $\Delta\Sigma$  modulators and tenfold oversampling has been considered in detail as a design example. The system has been shown to achieve 18-b A/D conversion performance under the assumption of ideal circuit behavior, and 16-b A/D conversion performance with 0.1% gain matching errors.

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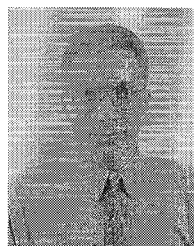
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