

NOISE-SHAPING D/A CONVERTERS FOR $\Delta\Sigma$ MODULATION

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ABSTRACT

Delta-sigma ($\Delta\Sigma$) data converters are highly sensitive to any signal-band conversion noise introduced by their internal DACs. To circumvent this problem, multi-bit DACs recently have been developed that use digital techniques to cause the conversion noise to reside primarily outside the signal-band. Such noise-shaping DACs have the potential to significantly increase the present precision limits of $\Delta\Sigma$ data converters. This paper extends the practicality of the approach by presenting extremely hardware-efficient 1st and 2nd-order noise-shaping multi-bit DACs. A simple theoretical explanation of the conversion noise-shaping phenomenon is also provided.

1. INTRODUCTION

In $\Delta\Sigma$ data conversion a coarse DAC is required in the processing chain but high-precision data conversion is performed by the overall system [1]. In most cases, the signal-band portion of the conversion noise introduced by the coarse DAC is not attenuated by the processing chain, so it directly degrades the overall signal to noise ratio (SNR) and spurious-free dynamic range (SFDR) of the data converter. For this reason, it has been common practice to use single-bit DACs in $\Delta\Sigma$ data converters. To the extent that errors in the two output levels of a single-bit DAC are static (time-invariant), the DAC only introduces constant gain and offset errors which do not reduce the SNR or SFDR of the $\Delta\Sigma$ data converter. Unfortunately, this requires single-bit $\Delta\Sigma$ modulators which suffer from performance-limiting effects such as reduced input range, conditional stability, and spurious tonal behavior.

Recently, various innovative multi-bit DAC architectures have been proposed for which the conversion noise is spectrally shaped like quantization noise in $\Delta\Sigma$ modulators [2]–[5]. Thus, when used in $\Delta\Sigma$ data converters, the same filters that remove much of the quantization noise also remove much of the DAC conversion noise. Remarkably, the architectures employ digital algorithms to perform this noise-shaping of errors introduced by non-ideal analog circuit behavior and the algorithms require no specific knowledge of the particular analog errors that are introduced.

The noise-shaping DACs represent exciting developments because they promise to greatly advance the present precision limits of $\Delta\Sigma$ data converters by eliminating the need for one-bit quantization. To date, 1st-order [3], [4] and 2nd-order [5] noise-shaping DAC architectures have been demonstrated in the literature via simulation results. However, the only architecture of these that achieves greater than 1st-order noise-shaping requires clock-rate digital number sorting, and therefore has a high implementation complexity. Moreover, no theory or detailed quantification of the performance of

any of the architectures has yet been published to the knowledge of this author.

This paper presents a hardware-efficient topology that can be used to achieve arbitrary conversion noise-shaping characteristics and presents specific 1st and 2nd-order noise-shaping DACs as special cases of the topology. The 2nd-order DAC, in particular, is considerably more hardware efficient than its previously presented counterpart. Expressions that characterize the conversion noise are also presented along with an overview of their derivation (the full analysis is presented in [6]).

2. THE DAC TOPOLOGY

The noise-shaping DAC topology presented in this paper is shown in Fig. 1. For simplicity, a 3-bit version is shown, but the topology and all of the results in this paper are easily generalized to any number of bits (the DAC shown in Fig. 1 is actually a 9-level DAC because there are 8 unit DAC-elements, so its input is slightly wider than 3-bits). The DAC consists of a digital portion, collectively referred to as the *digital encoder*, and N one-bit DACs referred to as *unit DAC-elements*. Each digital input sample, $x[n]$, is assumed to be an integer in the set $\{0, 1, \dots, 8\}$. The digital encoder consists of three *layers* of devices called *switching blocks* and labeled $S_{k,r}$, where k denotes the layer number and r denotes the position of the switching block in the layer. The details of the switching blocks will be described shortly, but at the high level of Fig. 1, each digital input sample, $x[n]$, is mapped by the digital encoder to 8 bits that satisfy

$$x_1[n] + x_2[n] + \dots + x_8[n] = x[n]. \quad (1)$$

The unit DAC-elements operate according to:

$$y_r[n] = \begin{cases} 1 + e_{h,r}, & \text{if } x_r[n] = 1; \\ e_{l,r}, & \text{if } x_r[n] = 0; \end{cases} \quad (2)$$

where $y_r[n]$ denotes the analog output of the r^{th} unit DAC-element, and $e_{h,r}$ and $e_{l,r}$ are errors in the analog output levels. Because the digital encoder implements (1), if these errors were all zero then the output of the DAC, $y[n]$, would equal the input, $x[n]$, exactly. However, in practice the errors are not zero because of non-ideal circuit behavior, so

$$y[n] = \alpha x[n] + \beta + e[n],$$

where α is a *constant gain*, β is a *DC offset*, and $e[n]$ is zero-mean *conversion noise*. Throughout the paper, $e_{h,r}$ and $e_{l,r}$ are assumed to be time-invariant, but otherwise arbitrary, and are referred to as *static mismatch errors*.

It can be easily verified that the digital encoder will satisfy (1) provided each switching block satisfies the following *number conservation rule*: *The two outputs of*

each switching block must be in the range $\{0, 1, \dots, 2^{k-1}\}$ where k is the layer number, and their sum must equal the input to the switching block. For example, if $x[n_0] = 6$, then the number conservation rule is satisfied by the Layer 3 switching block if its two outputs at time n_0 are any of the following pairs: (3, 3), (4, 2) or (2, 4).

3. SUMMARY OF PERFORMANCE

The two specific noise-shaping DACs considered in this paper have the topology shown in Fig. 1 with switching blocks that satisfy the number conservation rule, but they differ in the details of how their switching blocks operate. As will be shown, the conversion noise from the two DACs is spectrally shaped in the same fashion that quantization noise is shaped in 1st and 2nd-order $\Delta\Sigma$ modulators, respectively.

Before presenting the details of the switching blocks and associated theory, simulation results will be presented. Fig. 2a shows simulation data representing the output PSDs of a conventional DAC (taken as a thermometer encoder followed by the 8 unit DAC elements), a 1st-order noise-shaping DAC, a 2nd-order noise-shaping DAC, and an ideal DAC, all driven by the same 3-bit third-order digital $\Delta\Sigma$ modulator with a sinusoidal excitation. All but the ideal DAC had the same set of static mismatch errors which were chosen from a Gaussian distribution with a standard deviation of 1% (different distributions would have yielded similar results). The PSDs are in units of dB relative to the nominal least-significant-bit (LSB) value of the DACs (this is also the step-size of the $\Delta\Sigma$ modulator).

No conversion noise was introduced by the ideal DAC, so the PSD of the ideal DAC output is equal to that of the 3-bit, third-order digital $\Delta\Sigma$ modulator output. Accordingly, the PSD consists of third-order shaped quantization noise with a discrete spectral frequency component corresponding to the sinusoidal excitation of the $\Delta\Sigma$ modulator. As expected from well-known $\Delta\Sigma$ modulator results, the quantization noise component decreases by 18 dB per octave decrease in frequency. Each of the PSDs associated with the other three DACs differs from that of the ideal DAC because of an additional component corresponding to the conversion noise. As is evident from Fig. 2a, for the conventional DAC this component gives rise to a flat noise-floor at about -45 dB with a considerable spurious tone content. For the 1st-order and 2nd-order DACs the component gives rise to noise-floors that decrease by 6 dB and 12 dB per octave decrease in frequency, respectively, with very little spurious tone content. Similar data are shown in Fig. 2b for a sinusoidal input of a different frequency, and in Fig. 2c for a sinusoidal input with an extremely small amplitude (not visible above the noise floor). In each case, the simulation data clearly support the assertions made above that the 1st-order and 2nd-order DACs give rise to 1st-order and 2nd-order shaped conversion noise, respectively. Fig. 2d shows attainable bit precisions versus oversampling ratios between 2 and 200 as obtained from integrating the data of Fig. 2c.

4. THE SWITCHING BLOCK DETAILS

From a signal processing point-of-view, the switching blocks associated with the two noise-shaping DACs

considered above perform the operations shown in Fig. 3. In each case $s_{k,r}[n]$ is a sequence generated within the switching block, and the differences between the two DACs lie only in the algorithms their switching blocks use to calculate $s_{k,r}[n]$.

It follows from the figure that

$$s_{k,r}[n] = x_{k-1,2r-1}[n] - x_{k-1,2r}[n]. \quad (3)$$

Because the sequence $s_{k,r}[n]$ determines the difference between the two outputs of the $S_{k,r}$ switching block, it follows that $s_{k,r}[n]$ must satisfy certain conditions for the number conservation rule to be satisfied. Specifically, it can easily be verified that if all the switching blocks have the form shown in Fig. 3 and, for every k and r , $s_{k,r}[n]$ satisfies:

$$s_{k,r}[n] = \begin{cases} \text{even if } x_{k,r}[n] \text{ is even;} \\ \text{odd if } x_{k,r}[n] \text{ is odd;} \end{cases} \quad (4)$$

and

$$|s_{k,r}[n]| \leq \min\{x_{k,r}[n], 2^k - x_{k,r}[n]\}, \quad (5)$$

then the switching blocks all satisfy the number conservation rule.

For a b -bit version of the DAC topology shown in Fig. 1 wherein all the switching blocks satisfy the number conservation rule with sequences $s_{k,r}[n]$ that satisfy (4) and (5), the constant gain, DC offset, and conversion noise can be written as

$$\alpha = 1 + \frac{1}{2^b} \sum_{i=1}^{2^b} (e_{h_i} - e_{l_i}), \quad \beta = \sum_{i=1}^{2^b} e_{l_i}, \quad (6)$$

and

$$e[n] = \sum_{k=1}^b \sum_{r=1}^{2^{b-k}} \Delta_{k,r} s_{k,r}[n], \quad (7)$$

where

$$\Delta_{k,r} = \frac{1}{2^k} \sum_{i=(r-1)2^k+1}^{(r-1)2^k+2^k-1} [(e_{h_i} - e_{l_i}) - (e_{h_{i+2^k-1}} - e_{l_{i+2^k-1}})]. \quad (8)$$

The proof of this result is presented in [6] and sketched in the next section. Notice, in particular, that $\Delta_{k,r}$ is a constant that depends only upon the static mismatch errors. Consequently, it follows from (7) that if each switching block calculates $s_{k,r}[n]$ as an L^{th} -order shaped sequence that satisfies (4) and (5) and is uncorrelated from the $s_{k,r}[n]$ sequences of the other switching blocks, then the conversion noise will be an L^{th} -order shaped sequence.

The block diagrams shown in Fig. 4 indicate the signal processing operations performed by the switching blocks to generate $s_{k,r}[n]$ in the 1st-order and 2nd-order DACs considered above. Together with the structure in Fig. 3, the structures in Figures 4a and 4b represent the signal processing operations performed by the complete $S_{k,r}$ switching block for the 1st-order and 2nd-order DACs, respectively.

The $S_{k,r}$ switching block associated with the 1st-order DAC generates $s_{k,r}[n]$ as shown in Fig. 4a. The structure differs from a 1st-order $\Delta\Sigma$ modulator only in that it has no signal input and the hard limiter is followed by an LSB-multiplier that forces $s_{k,r}[n]$ to be zero whenever the LSB of the input to the switching block is zero (i.e., when the input is even). The $S_{k,r}$ switching block associated with the 2nd-order DAC generates $s_{k,r}[n]$ as shown in Fig. 4b. The structure is similar to a 2nd-order $\Delta\Sigma$ modulator. The quantizer has a step-size of $\Delta_q = 2$ and performs midtread quantization when the LSB of the input to the switching block is 0 and midrise quantization otherwise. The amplitude limiter clips the output of the quantizer, if necessary, to force $s_{k,r}[n]$ to satisfy (5).

For integer initial conditions, the state variables of the structures of Fig. 4 are always bounded integer values. Consequently, they can be implemented with low bit-width registers and arithmetic. For example, a gate-level implementation of the full switching block for the 1st-order DAC is shown in Fig. 5.

5. SKETCH OF THE THEORY

A functionally equivalent version of the DAC topology of Fig. 1 is shown in Fig. 6a from which the recursive nature of the system is evident. Each subsystem enclosed in a dashed box is a DAC in its own right and thus is referred to as $DAC_{k,r}$ where k and r are the indices of the left-most switching block in $DAC_{k,r}$. The recursive form of $DAC_{k,r}$ in terms of $DAC_{k-1,2r-1}$ and $DAC_{k-1,2r}$ is shown in Fig. 6b.

It is convenient to temporarily redraw the recursive DAC structure of Fig. 6b using the simplified notation shown in Fig. 7. The boxes labeled S , DAC_1 , and DAC_2 in Fig. 7 correspond to those labeled $S_{k,r}$, $DAC_{k-1,2r-1}$, and $DAC_{k-1,2r}$ in Fig. 6b. With this simplified notation, (3) and the number conservation rule imply

$$s[n] = x'_1[n] - x'_2[n], \quad \text{and} \quad x'[n] = x'_1[n] + x'_2[n], \quad (9)$$

respectively.

From a signal processing point-of-view, any non-ideal DAC can be viewed as a device that introduces a constant gain, a DC offset, and zero-mean conversion noise. For convenience in the derivation that follows, the DC offset and zero-mean conversion noise are lumped together and referred to as *additive noise*. Thus, the outputs of the two DACs in Fig. 7 can be written as

$$y'_i[n] = \alpha_i x'_i[n] + \epsilon_i[n] \quad (10)$$

for $i = 1$ and $i = 2$, where α_i and $\epsilon_i[n]$ are the gain and additive noise, respectively, associated with DAC_i .

From (10) and Fig. 7 it follows that

$$y'[n] = \alpha_1 x'_1[n] + \alpha_2 x'_2[n] + \epsilon_1[n] + \epsilon_2[n].$$

By applying (9), and collecting terms, this becomes

$$y'[n] = \alpha x'[n] + \epsilon[n], \quad (11)$$

where

$$\epsilon[n] = s[n]\Delta + \epsilon_1[n] + \epsilon_2[n], \quad (12)$$

$$\alpha = \frac{\alpha_1 + \alpha_2}{2}, \quad \text{and} \quad \Delta = \frac{\alpha_1 - \alpha_2}{2}. \quad (13)$$

Equation (12) indicates that the conversion noise of the recursive DAC of Fig. 7 consists of the conversion noise introduced by its two component DACs and a component arising from the mismatch between the gains of its component DACs. Suppose that Fig. 7 corresponds to $DAC_{1,1}$ in Fig. 6a. That is, suppose S , DAC_1 , and DAC_2 in Fig. 7 correspond to $S_{1,1}$ and the 1st and 2nd unit DAC-elements in Fig. 6a, respectively. From (10) and the definition of the static mismatch errors, it is easily verified that for this case $\alpha_i = 1 + e_{n_i} - e_i$ and $\epsilon_i[n] = e_i$ for $i = 1$ and $i = 2$ so the additive noise from each unit DAC-element is just a DC offset. Consequently, from (12) it follows that the only non-constant component of the additive noise introduced by $DAC_{1,1}$ is contributed by the term $s[n]\Delta$. But Δ is a constant, so if $s[n] = s_{1,1}[n]$ is an L^{th} -order shaped sequence, it follows that the conversion noise will be an L^{th} -order shaped sequence regardless of the values of the static mismatch errors. Clearly, the same argument applies to $DAC_{1,2}$, $DAC_{1,3}$, and $DAC_{1,4}$ in Fig. 6a.

Now suppose that Fig. 7 corresponds to $DAC_{2,1}$. By the argument made above, provided $s_{1,1}[n]$ and $s_{1,2}[n]$ are uncorrelated L^{th} -order shaped sequences, then the sum of the second two terms in (12) will also be an L^{th} -order shaped sequence. Consequently, provided $s[n] = s_{2,1}[n]$ is an L^{th} -order shaped sequence that is uncorrelated with $s_{1,1}[n]$ and $s_{1,2}[n]$, then $\epsilon[n]$, or, equivalently, the conversion noise introduced by $DAC_{2,1}$, is also an L^{th} -order shaped sequence. By induction, this argument applies to the entire DAC of Fig. 6a, and more generally to DACs of arbitrary size having the switching block topology wherein all the switching blocks satisfy the number conservation rule.

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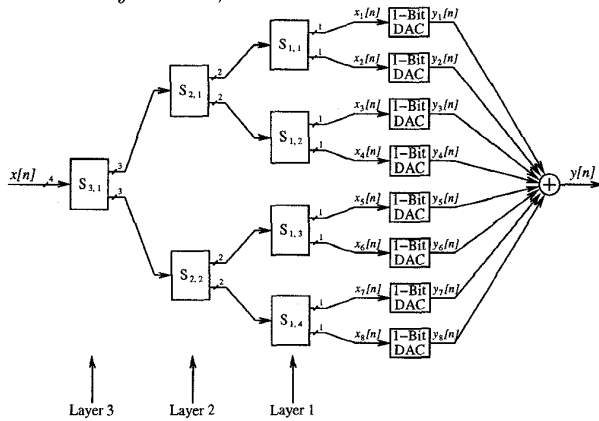


Figure 1: The high-level DAC topology.

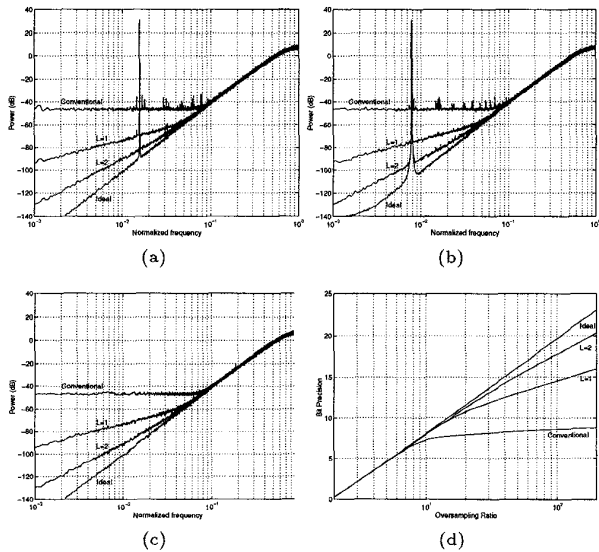


Figure 2: Simulation data: a)-c) PSDs of conventional, 1st-order, 2nd-order, and ideal DACs all driven by the same 3-bit third-order digital $\Delta\Sigma$ modulator, d) the corresponding bit precisions versus oversampling ratio.

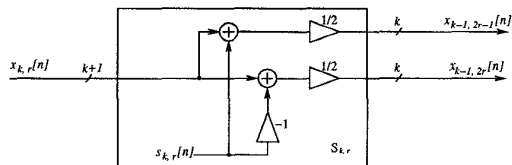


Figure 3: The general form of all the switching blocks.

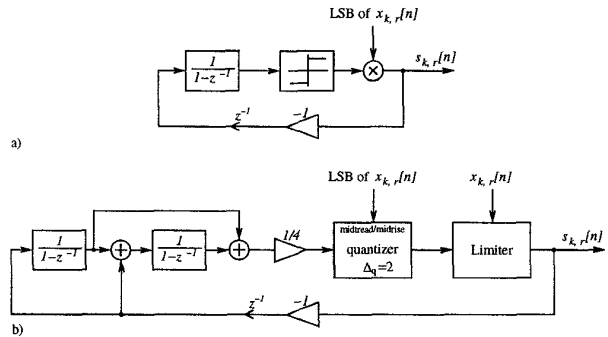


Figure 4: Calculation of $s_{k,r}[n]$ for the two DACs.

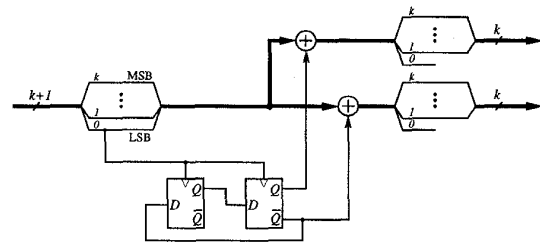


Figure 5: A hardware-efficient 1st-order switching block.

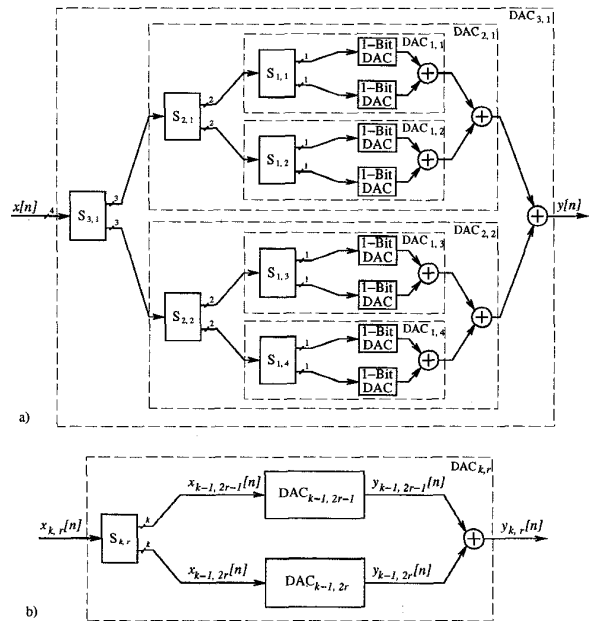


Figure 6: A redrawn but equivalent version of Fig. 1.

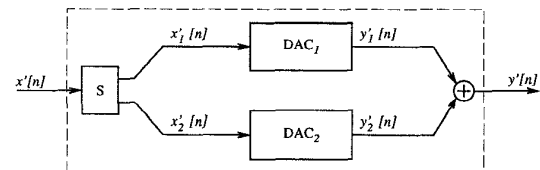


Figure 7: Fig. 6b drawn with simplified notation.