

# A HARDWARE-EFFICIENT DAC FOR DIRECT DIGITAL SYNTHESIS

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## ABSTRACT

This paper presents a new dynamic element matching technique for low harmonic distortion digital-to-analog converters suitable for direct digital synthesis systems. The benefit of the present approach over the prior art is significantly reduced hardware complexity with no reduction in performance.

## 1. INTRODUCTION

As a largely digital technique for generating high spectral-purity sinusoidal analog signals, direct digital synthesis (DDS) is increasingly used in wireless communications systems. The main limitation in any DDS system is imposed by the front-end DAC required to convert the digitally synthesized sinusoidal sequence into an analog waveform. In particular, non-ideal circuit behavior causes the DAC to introduce *conversion noise*. At least a component of the conversion noise is a non-linear function of the input sequence, so harmonic distortion is introduced that places an upper bound on the achievable spurious-free dynamic range (SFDR) of the overall system. As shown in [1] DDS applications typically require only moderate resolution (typically 5-12 bits) provided the harmonic distortion introduced by the DAC is small. For example, an extremely low-complexity 8-bit DDS system has been demonstrated that achieves a minimum SFDR of 90 dB provided the minimum SFDR of the DAC is 90 dB or greater.

Thus, a remaining problem is to develop moderate-resolution DACs that achieve such low levels of harmonic distortion. In the past, *dynamic element matching* (DEM) techniques have been successfully applied to decorrelate the conversion noise from the input signal in various DAC topologies. A particularly promising topology involves the use of a bank of 1-bit DACs, the outputs of which are summed together to yield a single multi-bit DAC [2], [3]. For most digital input values, there are many possible input codes to the bank of 1-bit DACs that nominally yield the desired analog output value. Thus, the conversion noise arising from errors introduced by the 1-bit DACs can be "scrambled" by randomly selecting one of the appropriate codes for each digital input value. Although DACs based on this approach have been shown experimentally and through quantitative analysis to achieve excellent SFDRs, the presented DACs suffer from excessive digital hardware complexity. For example, an 8-bit DAC based on the approach used in [2] requires 1024 binary switches and 1024 uncorrelated random control bits.

In this paper, a new DEM approach is presented that results in DACs with similar performance to those presented in [2] and [3], but with considerably lower hardware complexity. Two versions of the technique are

presented: *full randomization* DEM and *partial randomization* DEM. Theoretical results that quantify performance for the case of full randomization DEM are presented and closely supported by simulation results. Simulation results are also presented for the case of partial randomization DEM. The results show that full randomization DEM yields optimal SFDR performance, but partial randomization DEM yields very good SFDR performance. While both DEM versions have much lower hardware complexity than the previous comparable DEM approaches, the greatest hardware-efficiency is offered by the partial randomization version. For example, an 8-bit DAC based on the partial randomization DEM approach requires only 46 binary switches and 3 uncorrelated random control bits; with  $\pm 1\%$  static analog mismatch errors, the results indicate that the overall SFDR is greater than 90 dB.

## 2. DEM MULTI-BIT DAC APPROACHES

### 2.1. Background and Prior Art

The high-level topology of the DACs presented in [2] and [3] is shown in Fig. 1. The  $b$ -bit DAC consists of a *digital encoder* and  $2^b$  1-bit DACs referred to as *unit DAC-elements*. The digital input,  $x[n]$ , is a sequence of unsigned  $b$ -bit integers less than  $2^b$ . At the high level of Fig. 1, the digital encoder maps each input sample to  $2^b$  output bits such that  $\sum_{i=1}^{2^b} x_i[n] = x[n]$ . The unit DAC-elements operate according to

$$y_r[n] = \begin{cases} 1 + e_{h_r}, & \text{if } x_r[n] = 1; \\ e_{l_r}, & \text{if } x_r[n] = 0; \end{cases}$$

where  $y_r[n]$  denotes the analog output of the  $r^{\text{th}}$  unit DAC-element, and  $e_{h_r}$  and  $e_{l_r}$  are errors in the analog output levels. The errors are assumed to be time-invariant, but otherwise arbitrary, and are referred to as *static mismatch errors*. The  $r^{\text{th}}$  unit DAC-element is said to be *selected* whenever  $x_r[n] = 1$ .

With non-zero static mismatch errors, the output  $y[n]$  of the multi-bit DAC has the form

$$y[n] = \alpha x[n] + \beta + e[n]$$

where  $\alpha$  is a *constant gain*,  $\beta$  is a *DC offset*, and  $e[n]$  is zero-mean *conversion noise*. The purpose of the digital encoder is to dynamically select the unit DAC-elements such that  $e[n]$  is white and uncorrelated to the input. To accomplish this, the digital encoders of the prior art employ a *thermometer encoder* and a *scrambler*; the scrambler randomly maps its  $2^b$ -bit thermometer-code input to its  $2^b$ -bit output using a network of *binary switches*, each controlled by a *random control bit*.

## 2.2. Proposed DAC topology

The proposed DEM multi-bit DAC architecture is shown in Fig. 2. The DAC is of the general topology introduced in [4], and for simplicity a 3-bit example is shown in the figure. The digital encoder consists of three layers of *switching blocks*, each labeled  $S_{k,r}$ , where  $k$  denotes the layer number and  $r$  denotes the position of the switching block in the layer.

Fig. 3 shows the functional details of the switching block  $S_{k,r}$ . The switching block has one  $k + 1$ -bit input, two  $k$ -bit outputs, and an additional random control bit input,  $c_k[n]$ . The random control bit is common to all the  $S_{k,r}$  within the  $k^{\text{th}}$  layer, and, for clarity, is not shown in Fig. 2. Each  $c_k[n]$  is a white random bit-sequence, statistically independent of the random control bits used in the other layers.  $S_{k,r}$  operates such that when  $c_k[n]$  is high, the most significant bit (MSB),  $b_k$ , of the input is mapped to all  $k$  bits of the top output, and the remaining  $k$  bits of the input are mapped directly to the  $k$  bits of the bottom output. When  $c_k[n]$  is low, the situation is as above except that the mappings are interchanged. The process of randomly mapping the input to the outputs is referred to as *random switching*. At the outermost layer, i.e.,  $k = b$  ( $b = 3$  in Fig. 2), the DAC input  $x[n]$  is assigned to the  $S_{b,1}$  input bits  $b_1$  through  $b_b$ , and a zero is assigned to the input bit  $b_0$ , as indicated in Fig. 2.

Motivated by the performance details presented in the next section, two versions of the proposed architecture are now defined. The term *full randomization* DEM refers to a DAC with random switching in all layers, i.e., layers 1 through  $b$ . The term *partial randomization* DEM refers to a DAC with random switching in a limited number of layers, i.e., in layers  $r$  through  $b$ , where  $2 \leq r \leq b - 1$ .

As an example of partial randomization DEM, consider the 8-bit DAC of Fig. 4, where random switching is performed in layers 6 through 8. Since layers 1 through 5 have no effect on the randomness of the selection of the unit DAC-elements, it follows that these layers can be substituted by eight nominally identical *DAC banks*, each with a 6-bit input. The details of the DAC bank are shown in Fig. 5. The LSB of the input controls a unit DAC-element, whereas the remaining 5 bits control a 5-bit conventional DAC.

## 3. PERFORMANCE DETAILS

### 3.1. Full Randomization DEM

The simulated performance of an example 8-bit DAC with the proposed architecture is presented in Fig. 6. Each graph in the figure shows the estimated power spectral density (PSD) of a particular signal of the DAC operating with a dithered sinusoidal input. Fig. 6a corresponds to  $y[n]$  of an ideal DAC (no static mismatch errors), Fig. 6b corresponds to  $y[n]$  with no random switching (the digital encoder thus being equivalent to a thermometer encoder), Fig. 6c corresponds to the signal  $y[n] - x[n]$  with full randomization DEM, and Fig. 6d corresponds to  $y[n]$  with full randomization DEM. The static mismatch errors were chosen to within  $\pm 1\%$  of the nominal LSB value of the DAC. As is evident from the numerous spurs distributed across the spectrum in Fig. 6b, rather severe harmonic distortion results from

the static mismatch errors in the absence of random switching. The SFDR provided by the DAC is merely 68 dB. The data in Fig. 6d shows that harmonic distortion is not visible with full randomization DEM. The DAC easily provides 90 dB SFDR and is thus applicable to the DDS system mentioned in the Introduction. Numerically integrating the conversion noise component of the data in Fig. 6c yields a conversion noise power of  $-23.4$  dB relative to the nominal LSB value.

Further details of the simulation data are as follows. The PSDs were each estimated by averaging 16 length- $2^{18}$  periodograms. The input was generated by adding dither to a sinusoid of frequency  $\frac{625}{2048}\pi$  radians and quantizing to an 8-bit value. The dither was a white sequence with a triangular probability density function supported on  $(-1, 1)$ , so the quantization error was white noise.

A theoretical performance analysis of the proposed architecture is given in [5]. For the purposes of this presentation, the main result of the analysis will be stated here without proof, although the theoretical results will be supported by simulations.

In the following, let  $x^{(i)}[n]$  denote the  $i^{\text{th}}$  bit of the input  $x[n]$ , where  $0 \leq i \leq b - 1$ . In accordance with the usual definitions, let the time-average mean of  $x[n]$ ,  $x^{(i)}[n]$ , and  $x^{(i)}[n]x^{(j)}[n]$  be defined as

$$\overline{M}_x = \lim_{P \rightarrow \infty} \frac{1}{P} \sum_{n=1}^P x[n],$$

$$\overline{M}_{x^{(i)}} = \lim_{P \rightarrow \infty} \frac{1}{P} \sum_{n=1}^P x^{(i)}[n],$$

and

$$\overline{M}_{x^{(i,j)}} = \lim_{P \rightarrow \infty} \frac{1}{P} \sum_{n=1}^P x^{(i)}[n]x^{(j)}[n],$$

respectively, and let the time-average autocorrelation of  $x[n]$  be defined as

$$\overline{R}_{xx}(k) = \lim_{P \rightarrow \infty} \frac{1}{P} \sum_{n=1}^P x[n]x[n+k].$$

The time-average autocorrelation of  $y[n]$  is defined analogously with  $x$  replaced by  $y$  in the above definition. The main theoretical result of [5] can now be stated as follows: *If  $\overline{M}_x$  and  $\overline{R}_{xx}[k]$  exist, then*

$$\overline{R}_{yy}[k] = \alpha^2 \overline{R}_{xx}[k] + \overline{\eta} + \overline{\sigma}^2 \delta[k], \quad (1)$$

with probability 1, where

$$\alpha = 1 + \frac{1}{2^b} \sum_{i=1}^{2^b} (e_{h_i} - e_{l_i}),$$

$$\overline{\eta} = 2\alpha\beta\overline{M}_x + \beta^2,$$

and

$$\overline{\sigma}^2 = \sum_{i=0}^{b-1} \gamma_i \overline{M}_{x^{(i)}} + \sum_{j=0}^{b-2} \sum_{i=j+1}^{b-1} \gamma_{i,j} \overline{M}_{x^{(i,j)}}. \quad (2)$$

In the equations for  $\bar{\eta}$  and  $\bar{\sigma}^2$ ,

$$\beta = \sum_{i=1}^{2^b} e_{i_i},$$

$$\gamma_i = \frac{1}{2^{b-i}} \sum_{j=0}^{2^{b-i}-1} (w_{i,j})^2,$$

and

$$\gamma_{i,j} = \frac{1}{2^{b-j-2}} \sum_{k=0}^{2^{b-i-1}-1} w_{i,2k} w_{i,2k+1}$$

where

$$w_{k,l} = \sum_{m=l2^k+1}^{(l+1)2^k} (e_{h_m} - e_{l_m} - \alpha + 1).$$

This result is independent of the underlying statistical distribution or any correlation properties of the static mismatch errors.

In summary, (1) states that  $\bar{R}_{yy}[k]$  consists of a scaled version of  $\bar{R}_{xx}[k]$ , a DC offset and white conversion noise. This is supported by the data in Fig. 6c. In particular, evaluating (2) for the simulated values of static mismatch errors of the 8-bit example DAC yields  $\bar{\sigma}^2 = -23.4$  dB relative to the nominal LSB value, in agreement with the simulated data.

In [5], the above result is used to estimate fabrication yields as a function of the static mismatch error statistics.

### 3.2. Partial Randomization DEM

Simulation data for partial randomization DEM is shown in Fig. 7. In particular, Fig. 7a-c correspond to the signal  $y[n] - x[n]$  with random switching in layer 8, layers 7 and 8, and layers 6, 7, and 8, respectively. Fig. 7d corresponds to  $y[n]$  with random switching in layers 6, 7, and 8. As indicated by the data, the harmonic distortion is gradually attenuated as the number of layers with random switching is increased; the SFDRs of the plots are 72 dB, 78 dB, and 90 dB, respectively. The parameters for the computation of the PSD estimates were identical to the parameters used for Fig. 6.

For this example, three layers of random switching suffices to provide the desired 90 dB SFDR. Several simulations using other sinusoid frequencies and amplitudes similarly support this conclusion.

## 4. HARDWARE COMPLEXITY

An appropriate measure of the hardware complexity of the digital encoder is the required number of binary switches and the required number of random control bits. As will be quantified in the following, the proposed architecture has much lower hardware complexity than the prior art.

### 4.1. Full Randomization DEM

The required number of binary switches of the digital encoder of the proposed architecture is  $2^{b+1} - b - 2$ , and the required number of random control bits is simply  $b$ . As a comparison, the digital encoders presented in [2] and [3] require  $b2^{b-1}$  and  $(b - \frac{1}{2})2^b$  binary switches,

respectively, and the same number of random control bits as binary switches. It follows that the number of required random control bits has been reduced exponentially in  $b$ , whereas the number of required binary switches has been reduced linearly in  $b$  compared to the prior art. A detailed comparison of hardware complexity is shown in Fig. 8. The figure shows the hardware complexity of the architecture presented in [2] and the proposed architecture for bit-resolutions 6 through 12. The table entries are given as pairs  $(x/y)$ , where  $x$  is the required number of binary switches and  $y$  is the required number of random control bits.

### 4.2. Partial Randomization DEM

As indicated previously, even lower hardware complexity is achieved with partial randomization DEM. To obtain a precise count of the hardware, suppose that the digital encoder performs random switching in layers  $r$  through  $b$ . The required number of binary switches is then  $(r+1)2^{b-r+1} - b - 2$ . Of course, the required number of random control bits is  $b - r + 1$ . Thus, for the 8-bit example DAC with random switching in layers 6 through 8, the number of required binary switches reduces to  $7 \times 8 - 8 - 2 = 46$ . This should be compared to 502 for the case of full randomization DEM and 1024 for the prior art. To further illustrate the reduction of hardware complexity when partial randomization DEM is employed, Fig. 9 lists the hardware complexity of an 8-bit example DAC versus the range of layers with random switching.

## 5. CONCLUSION

A new hardware efficient DEM DAC architecture suitable for DDS has been presented. Compared to the prior art, the architecture is highly hardware efficient yet provides the same performance.

Quantitative results giving the conversion noise floor and allowing for a yield estimate were stated for the architecture with full randomization DEM. Computer simulations supporting the theoretical results were presented for an 8-bit example DAC.

As indicated by simulation results, using partial randomization DEM greatly suppresses harmonic distortion and has the benefit of considerable additional savings in hardware. Additional research is needed to theoretically quantify the performance with partial randomization DEM.

## REFERENCES

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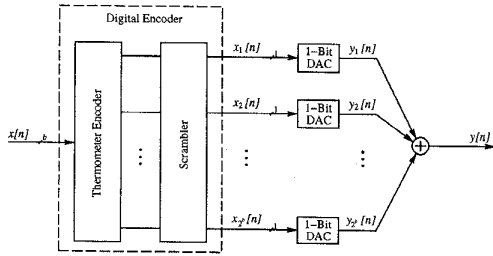


Figure 1: The high-level topology of the prior art.

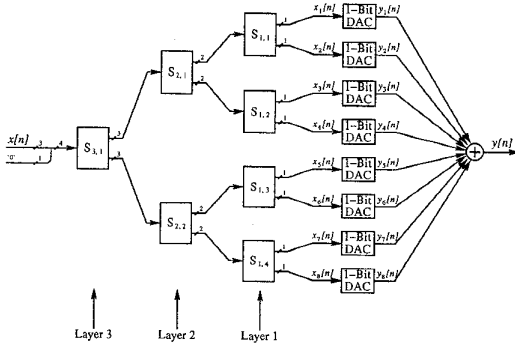


Figure 2: A 3-bit DAC of the proposed architecture.

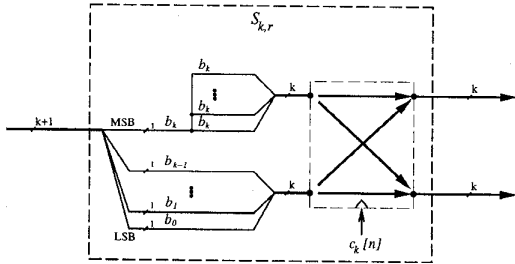


Figure 3: Details of the switching block  $S_{k,r}$ .

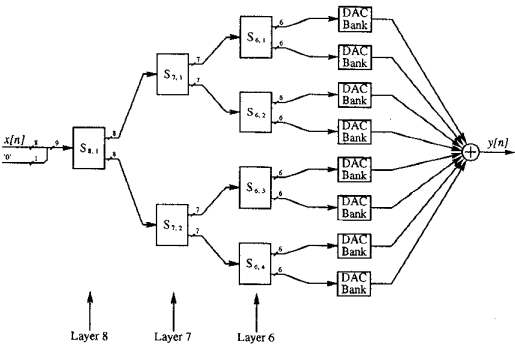


Figure 4: An 8-bit DAC with partial randomization DEM.

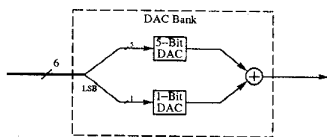


Figure 5: Details of the DAC bank.

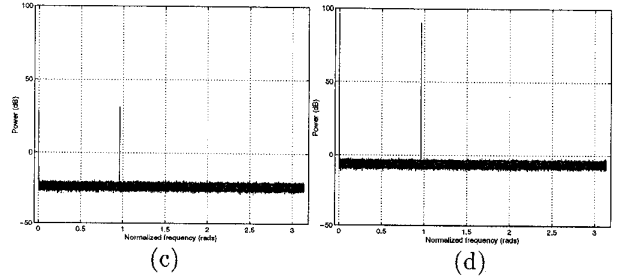
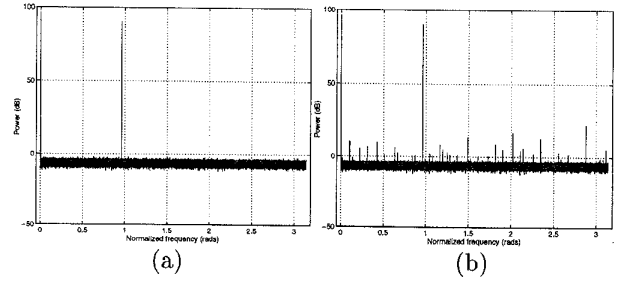


Figure 6: Estimated PSDs of the example 8-bit DAC.

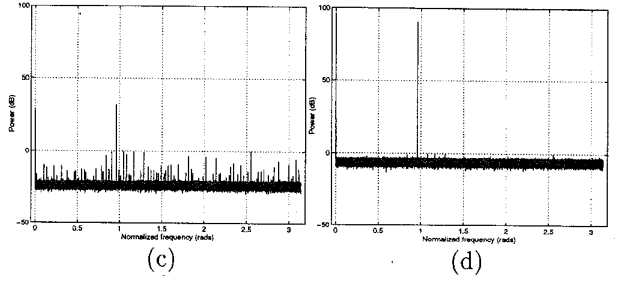
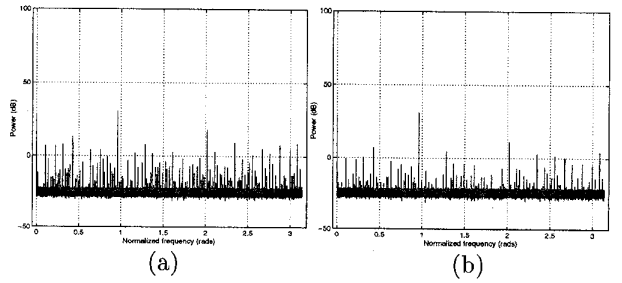


Figure 7: Estimated PSDs of the example 8-bit DAC with partial randomization DEM.

DAC Bits	6	7	8	9	10	11	12
Digital Encoder Reported in [2]	192 / 192	448 / 448	1024 / 1024	2304 / 2304	5120 / 5120	11264 / 11264	24576 / 24576
Proposed Digital Encoder	120 / 6	247 / 7	502 / 8	1013 / 9	2036 / 10	4083 / 11	8178 / 12

Figure 8: A comparison of hardware complexity.

Layers with Random Switching	8	7-8	6-8	5-8	4-8	3-8	2-8
Hardware Complexity	8 / 1	22 / 2	46 / 3	86 / 4	150 / 5	246 / 6	374 / 7

Figure 9: Hardware complexity of an 8-bit DAC with partial randomization DEM.