A Practical Second-Order Delta-Sigma Frequency-to-Digital Converter

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ABSTRACT

Digital phase-locked loops (DPLLs) that operate in an analogous fashion to delta-sigma ($\Delta\Sigma$) modulator A/D converters have been recently proposed. Although they offer certain advantages over conventional DPLLs, their direct implementation requires components that are difficult to realize without high-precision analog circuitry. This paper presents an alternate mechanization approach that gives rise to systems that have the same theoretical performance as those presented previously, but consist of easily implemented components such as analog integrators, digital flip-flops, and digital counters.

INTRODUCTION

The purpose of a DPLL is to generate a digital estimate of the instantaneous frequency of an angle-modulated analog input signal. Thus, a DPLL simultaneously performs the operations of an analog phase-locked loop and an A/D converter. With the trends toward digital communications and digital signal processing, DPLLs have increasingly replaced their analog counterparts as fundamental building blocks in coherent communication systems [1].

Nevertheless, practical DPLLs suffer from a problem not seen in their analog counterparts: performance degradation due to quantization. Conventional DPLLs are typically designed by initially neglecting the effects of quantization. Then, simulations or numerical analyses are used to determine the minimum acceptable quantization resolution for the particular DPLL architecture and application. Consequently, most DPLLs are not designed to minimize the error introduced by quantization, and quantization effects often limit their performance [2], [3].

Recently, DPLLs have been presented [4]–[7] that measure instantaneous frequency in an analogous fashion to the way that $\Delta\Sigma$ modulator A/D converters measure amplitude [8]. Although they use very coarse phase quantization, they avoid the deleterious effects suffered by other highly quantized DPLL architectures through the use of quantization noise shaping and lowpass filtering. The DPLLs presented in [4]–[6], which are referred to as $\Delta\Sigma$ frequency-to-digital converters ($\Delta\Sigma$FDCs), have the additional benefit that their outputs can be summed modulo-2π to obtain an accurate phase modulation estimate that is appropriate for demodulation of phase-coherent communication signals such as minimum shift keying (MSK) signals [6].

Although the $\Delta\Sigma$FDCs as presented in [4]–[6] are conceptually simple, they require phase detectors and digitally controlled oscillators that can be difficult to implement accurately without high-precision analog circuitry [1]. This paper presents an alternate mechanization approach that gives rise to $\Delta\Sigma$FDCs that have the same theoretical performance as those presented previously, but consist of easily implemented components such as analog integrators, digital flip-flops, and digital counters.

BACKGROUND

Each $\Delta\Sigma$FDC is designed to generate a digital estimate of the instantaneous frequency modulation, $\phi(t)$, about a fixed center frequency, f_c, from which an accurate digital estimate of the phase modulation, $\theta_x(t)$, can be calculated up to an additive constant using modulo-2π accumulation. The assumed input signal is

$$x_r(t) = A\sin\big(2\pi f_c t + \theta_x(t)\big),$$

where A is a constant amplitude.

$$\theta_x(t) = 2\pi\int_{t_{n_0}}^{t}\phi(\tau)d\tau + \theta_0,$$

and θ_0 is an arbitrary initial value of $\theta_x(t)$ at time t_{n_0}.

As depicted in Figure 1, a $\Delta\Sigma$FDC consists of a modulator loop and a lowpass digital filter. The modulator loop operates on $x_r(t)$ and produces a digital output, $y[n]$, that is a coarsely quantized digital representation of $\phi(t)$. The sample-rate of $y[n]$ is much higher than the bandwidth of $\phi(t)$, so the component of $y[n]$ corresponding to $\phi(t)$ occupies primarily a low-frequency band. However, the component of $y[n]$ corresponding to quantization error occupies primarily a high-frequency band. Therefore, the lowpass filter is able to remove the out-of-band portion of the quantization error without significantly distorting the component associated with $\phi(t)$.

A second-order modulator loop is shown in Figure 2a [5]. It consists of a modulator-front-end (MFE) subsystem (to be described), a discrete-time integrator, a three-level A/D converter, and a digital feedback transfer function of $2 - z^{-1}$. As shown in [5], the MFE can be designed such that the modulator loop operates on a sampled representation of $\phi(t)$ as the scaled second-order $\Delta\Sigma$ modulator shown in Figure 2b. In particular, if the sampled representation of $\phi(t)$ is defined as:

$$\widehat{\phi}[n] = \int_{t_{n-1}}^{t_n}\phi(\tau)d\tau, \qquad (1)$$

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where $\{t_n\}$ is the sequence of sample times of $y[n]$, then the modulator loop is equivalent to Figure 2b provided the MFE realizes the following equation:

$$d[n] = K_p K_v T_s \sum_{k=n_0+1}^{n} \left(\frac{1}{K_v T_s} \widehat{\phi}[k] - v[k-1] \right) + \alpha, \quad (2)$$

where K_p, K_v, T_s, and α are constants. In this case, the $\Delta\Sigma$FDC generates an output of the form

$$h[n] * \left[\frac{1}{K_v T_s} \widehat{\phi}[n] + e_2[n] \right],$$

where $h[n]$ is the lowpass filter impulse response, and $e_2[n]$ is equivalent to the noise introduced by the A/D converter passed through the second-order highpass filter $N(z) = (1 - z^{-1})^2$. If the output of the $\Delta\Sigma$FDC is scaled by $2\pi K_v T_s$ and accumulated modulo-2π, the resulting estimate of $\theta_x(t_n)$ has the form [6]

$$\left\{ h[n] * \left[\theta_x(t_n) + \theta_0' + 2\pi K_v T_s e_1[n] \right] \right\} \bmod 2\pi$$

where θ_0' is a constant, and $e_1[n]$ is equivalent to the noise introduced by the A/D converter subjected to the filter $(1 - z^{-1})$. Because of the oversampling, the lowpass filter has little effect on the $\theta_x(t_n)$ term. However, the high frequency quantization error is significantly attenuated and can be calculated using standard $\Delta\Sigma$ modulator results [8].

THE PROPOSED MECHANIZATION

This section presents a practical mechanization of the modulator loop shown in Figure 2a. Like the majority of DPLL mechanizations [1], it is based on a non-uniform sampling scheme. Provided the digital filter and modulo-2π accumulator are clocked at the non-uniform sampling instants, the theory outlined above remains valid.

Figure 3 shows a block diagram of the proposed modulator loop mechanization. As will be shown, the structure implements the modulator loop of Figure 2a, because the subsystem within the dashed box is functionally equivalent to an MFE followed by a discrete-time integrator. The system uses a hard limited version of the input signal to clock a D flip-flop whose data input is always high. The flip-flop is cleared on the rising edge of a signal, $s(t)$, that is generated as the carry bit of a digital up-counter. A scaled version of $s(t)$ is subtracted from the output of the flip-flop and the result is integrated and sampled-and-held on the rising edge of $s(t)$. The output of the sample-and-hold is scaled by $(K_p K_v T_s)^{-1}$ (these parameters will be derived below), and A/D converted to a three-level digital sequence.

To show that the modulator loop of Figure 3 is functionally equivalent to that of Figure 2a, it is sufficient to show that the subsystem within the dashed box of Figure 3 operates as an MFE followed by a discrete-time integrator. That is, it is sufficient to show that

$$q'[n] = \sum_{k=n_0+1}^{n} d[k] + q'[n_0], \quad (3)$$

where $d[n]$ has the form of (2) for some, as yet to be determined, constants K_p, K_v, T_s and α. To this end, the following definitions are useful:

1) $\tau_{n_0}, \tau_{n_0+1}, \tau_{n_0+2}, \ldots$, are the times of the rising edges of $s(t)$,
2) $t_{n_0}, t_{n_0+1}, t_{n_0+2}, \ldots$, are the times of the rising edges of the Q-output of the D flip-flop labeled such that $\ldots, t_{n-1} < \tau_{n-1} < t_n < \tau_n < t_{n+1} < \tau_{n+1}, \ldots$,
3) for each n, $q[n]$, $y[n]$, and $v[n]$ all correspond to the time interval $\tau_n \le t < \tau_{n+1}$,
4) the logical high and low levels of the Q-output of the D flip-flop are V_h and 0, respectively, and
5) $T_s = 1/f_c$.

The up-counter is clocked at a rate $f_m = M f_c$ where M is a positive integer. It operates as a variable-period pulse generator. When the counter reaches its terminal value of $2M - 1$, the carry bit (and, therefore, $s(t)$) goes high. On the next rising edge of the f_m-rate clock, the counter is loaded with the value $M + v[n-1]/\Delta$. The factor of $1/\Delta$ arises because it is customary to consider the LSB of a counter to be unity, but in this case the LSB of the counter corresponds to that of the A/D converter which has an implicit value of Δ (assuming mid-tread quantization).

Thus,

$$(2M - 1) - (M + v[n-1]/\Delta) + 1 = M - v[n-1]/\Delta$$

time intervals of duration $1/f_m = T_s/M$ separate τ_n and τ_{n-1}. With the definition that $\Delta_n = \tau_n - \tau_{n-1}$, it follows that

$$\Delta_n = T_s \left[1 - \left(\frac{1}{\Delta M} \right) v[n-1] \right]. \quad (4)$$

From Figure 3, it follows that

$$q'[n] = \int_{\tau_{n_0}}^{\tau_n} w(\tau) d\tau + q'[n_0].$$

This can be rewritten as (3) with the definition that

$$d[n] = \int_{\tau_{n-1}}^{\tau_n} w(\tau) d\tau. \quad (5)$$

Therefore, it remains to show that (5) is equivalent to (2) for some constants K_p, K_v, and α.

Figure 4 shows typical plots of the signals $w(t)$ and $s(t)$. From the figure and (5), it follows that

$$d[n] = V_h(\tau_n - t_n) - \gamma A_p T_p, \quad (6)$$

where A_p and T_p are the amplitude and duration, respectively, of the pulses in $s(t)$. To make further progress, expressions are required for τ_n and t_n in terms of $v[n]$ and $\widehat{\phi}[n]$.

An expression for τ_n is most easily derived from (4). By definition,

$$\tau_n = \sum_{k=n_0+1}^{n} \Delta_k + \tau_{n_0}.$$

Expanding Δ_k using (4) leads to

$$\tau_n = \sum_{k=n_0+1}^{n} T_s\left[1 - \left(\frac{1}{\Delta M}\right)v[k-1]\right] + \tau_{n_0}. \quad (7)$$

To determine an expression for t_n, assume that after time τ_{n_0-2} the A/D converter has not overloaded (i.e., $|q[n]| < 3\Delta/2$ for all $n > n_0 - 2$). In this case, the modulator loop is said to be in tracking mode and the positive going zero crossings of $x_r(t)$ occur at times t_n. The phase, in radians, of $x_r(t)$ can be written as $p_x(t) = 2\pi f_c t + \theta_x(t)$. Therefore,

$$p_x(t_n) = p_x(t_{n-1}) + 2\pi f_c \delta_n + 2\pi\widehat{\phi}[n], \quad (8)$$

where $\delta_n = t_n - t_{n-1}$. By the definition of t_n, it follows that $p_x(t_n) - p_x(t_{n-1}) = 2\pi$, so (8) can be rearranged as $\delta_n = T_s(1 - \widehat{\phi}[n])$. By definition,

$$t_n = \sum_{k=n_0+1}^{n} \delta_k + t_{n_0},$$

so

$$t_n = \sum_{k=n_0+1}^{n} T_s(1 - \widehat{\phi}[k]) + t_{n_0}. \quad (9)$$

Substituting (7) and (9) into (6) results in

$$d[n] = V_h\left[T_s\sum_{k=n_0+1}^{n}\left(\widehat{\phi}[k] - \frac{v[k-1]}{\Delta M}\right) + \tau_{n_0} - t_{n_0}\right] - \gamma A_p T_p.$$

With the definitions:

$$K_p = V_h T_s, \qquad K_v = \frac{1}{\Delta M T_s},$$

and

$$\alpha = \frac{K_p}{T_s}(\tau_{n_0} - t_{n_0}) - \gamma A_p T_p,$$

this reduces to (2) as required.

It remains to select values for the scale factor γ and for the parameter M. Notice from the expressions for K_p, K_v, and α that γ only appears in the expression for α. At first glance, one might be tempted to eliminate the circuitry associated with γ in Figure 3, effectively setting $\gamma = 0$. However, to do so would be catastrophic. The derivation above assumes that the modulator loop has been in tracking mode since time τ_{n_0}. It is apparent from (6) that if γ were zero then $d[n]$ would always have the same sign as V_h. But $d[n]$ is integrated prior to A/D conversion, so the magnitude of the A/D converter input would grow without bound and instability would result (thereby violating the assumption that the modulator loop is in tracking mode).

To avoid this problem, γ must be chosen to "bias" (6) so that $d[n]$ can attain both positive and negative values. In particular, γ must be chosen so that the range of possible values of the right-side of (6) contains the maximum operating range of $d[n]$. Provided this restriction is satisfied, the precise value of γ is not critical with respect to tracking mode because it only affects the initial state of the MFE. However, for maximum noise immunity it is preferable to bias (6) so that the range of values it can assume is symmetric about zero.

The worst-case range of (6) occurs when the separation between t_{n+1} and t_n is at its minimum. For the worst-case range to be symmetric about zero, $d[n]$ must equal zero when τ_n is midway between minimally separated values of t_{n+1} and t_n. From (6), this occurs when

$$\gamma = \frac{V_h \delta_{\min}}{2A_p T_p},$$

where $\delta_{\min}$ is the minimum separation between t_{n+1} and t_n.

If the instantaneous frequency excursion of $x_r(t)$ is restricted such that $|\widehat{\phi}[n]| < \beta$ for some constant β (which requires $|\phi(t)| < \beta/T_s(1-\beta)$) then $\delta_{\min} = T_s(1-\beta)$. Thus, with this choice of γ, the maximum (worst case) range of (6) is

$$|d[n]| \le V_h T_s(1-\beta)/2. \quad (10)$$

A standard linear system analysis of Figure 2a [6] shows that, during tracking mode,

$$|d[n]| \le 2K_p\beta + 3K_pK_vT_s\Delta. \quad (11)$$

Thus, M must be chosen sufficiently large that the right side of (10) is larger than that of (11). Simulations (one of which is described below) indicate that provided $\beta = 0.4K_vT_s\Delta$, then the A/D converter rarely overloads. With β so chosen, the above-mentioned inequality becomes

$$V_hT_s(1 - 0.4K_vT_s\Delta)/2 \ge 3.8K_pK_vT_s\Delta.$$

Substituting the expressions derived above for K_p and K_v and solving for M gives $M \ge 8$. Hence, the master clock frequency must satisfy $f_m \ge 8f_c$ for proper tracking mode operation.

SIMULATION RESULTS

Figure 5 shows simulation data corresponding to the system of Figure 3 with $M = 8$, $V_h = 1$, and $\phi(t) = 0.29985K_vT_s\Delta$. Figure 5a shows the estimated power spectral density (PSD) of the quantization error, and Figure 5b shows the corresponding in-band quantization error versus oversampling ratio calculated from the data in Figure 5a. The simulation was performed at the block diagram level of Figure 3 using

Simulink [9]. The Runge-Kutta 23 integration method was used with a minimum step-size of $1/(20f_m)$. The spectral estimation was performed by averaging five periodograms corresponding to non-overlapping Hanning windowed length-8192 segments of the simulated modulator loop output. The in-band quantization error power was calculated by integrating the in-band portion of the PSD. As is evident from the figure, the simulated modulator loop performs as predicted by theory. For example, Figure 5b indicates that for each doubling of the oversampling ratio the in-band quantization error power (i.e., the power of that portion of the quantization error residing within the frequency range $(-\pi/N, \pi/N)$ where N is the oversampling ratio) from the modulator loop decreases by 15 dB. This corresponds to an increase in digital conversion precision of 2.5 bits. An irrational input was used because, as in the case of $\Delta\Sigma$ modulators, rational dc inputs would have given rise to discrete tones in the quantization error. Alternatively, dithering could have been used to achieve similar quantization error data for any independent input sequence that does not result in overload.

ACKNOWLEDGMENT

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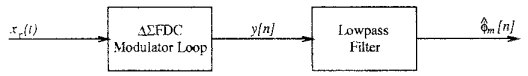

Figure 1: The high-level structure of a $\Delta\Sigma$FDC.

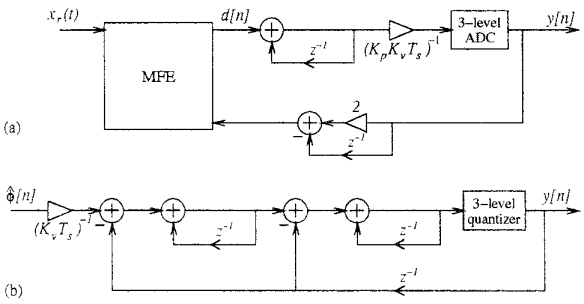

Figure 2: a) A second-order modulator loop. b) The equivalent $\Delta\Sigma$ modulator.

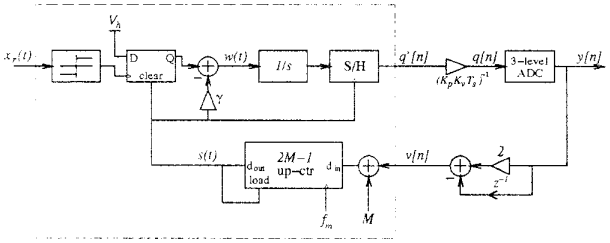

Figure 3: The proposed mechanization.

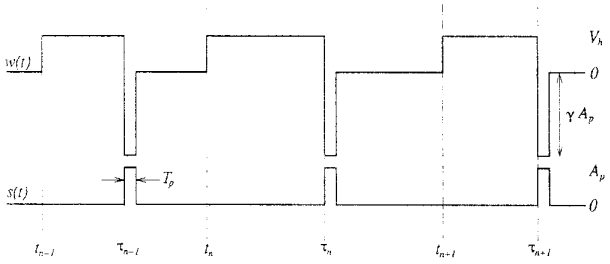

Figure 4: Typical plots of $w(t)$ and $s(t)$.

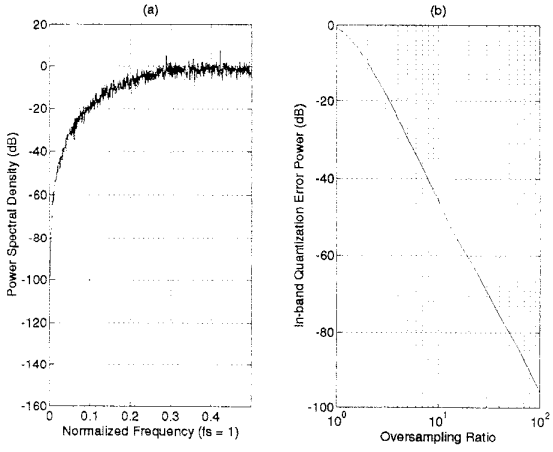

Figure 5: Simulation data: a) quantization error PSD b) in-band quantization error power.