Parallel Delta-Sigma A/D Conversion[1]

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Abstract

This paper presents an architecture wherein multiple delta-sigma modulators are combined so that neither time oversampling nor time interleaving are necessary. For a system containing M Pth-order delta-sigma modulators, approximately P bits of accuracy are gained for every doubling of M. Thus, the resolution gained by combining M delta-sigma modulators is approximately the same as that with the same modulator with an oversampling rate of M. Measured results from a 16-channel parallel delta-sigma A/D converter composed of second-order delta-sigma modulators verify the theory and demonstrate that this architecture retains much of the robustness of the individual delta-sigma modulators to non-ideal circuit behavior.

I. The Parallel $\Delta\Sigma$ A/D Converter Architecture

The parallel delta-sigma ($\Pi\Delta\Sigma$) A/D converter architecture is shown in Fig. 1 [1,2]. The analog input $x(n)$ is simultaneously applied to M modulators each followed by a conventional delta-sigma modulator. The $\Delta\Sigma$ modulator outputs are then filtered, demodulated and summed together to produce a single digital output sequence. In the conventional $\Delta\Sigma$ A/D converter both the signal and quantization noise pass through the same filter and therefore, both are filtered by the lowpass decimation filter, Fig. 2(a). In contrast, the $\Pi\Delta\Sigma$ A/D converter filters out much of the quantization error contributed by the $\Delta\Sigma$ modulators without filtering the input signal and without oversampling, Fig. 2(b).
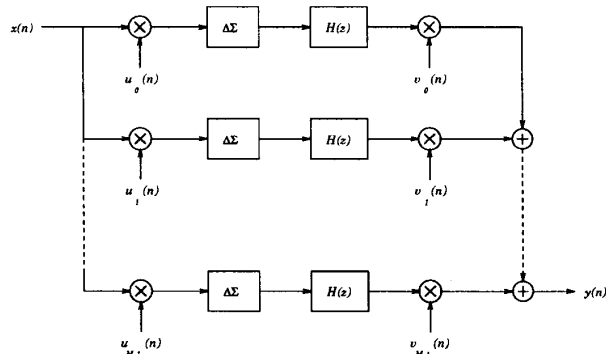

Figure 1: The parallel delta-sigma architecture.

The sequences $u_r(n)$, $0 \leq r \leq M - 1$, are referred to as Hadamard sequences and the process of multiplying by a Hadamard sequence is referred to as Hadamard modulation. The Hadamard modulation is especially well suited for implementation since it consists solely of plus and minus ones. Thus depending on the value of the Hadamard sequence, the analog input signal and the digital output sequence are either passed or inverted.
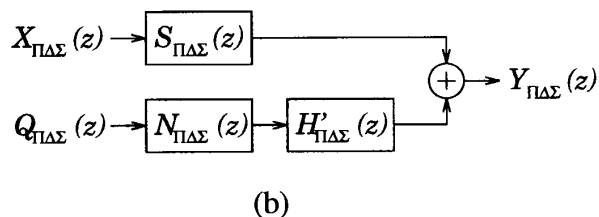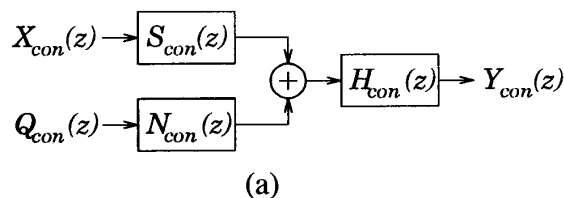

Figure 2: The signal and quantization signal paths for (a) the conventional delta-sigma modulator and (b) the parallel delta-sigma modulator.

For a given number of channels (M), filter length and $\Delta\Sigma$ modulator, the power of the overall quantization error component can be determined using Fig. 3. For example, for a thiry-two channel $\Pi\Delta\Sigma$ A/D converter with third-order $\Delta\Sigma$ modulators, and filters of length-190 or greater, Fig. 3 indicates that P_e is 81 dB below Δ^2 where Δ is the quantizer step size and P_e is the power in the quantization. To calculate the minimum number of bits, R, that a uniform quantizer A/D converter would require to achieve the same mean squared A/D conversion error as the $\Pi\Delta\Sigma$ A/D converter, we use the approximate formula [5]

$$R = \frac{1}{2}\log_2 \frac{\gamma^2}{3P_e}, \tag{1}$$

where γ is the maximum absolute value of the $\Pi\Delta\Sigma$ modulator input sequence. For $\Delta = 1$ and $\gamma = 0.3$, the conversion accuracy of the $\Pi\Delta\Sigma$ A/D converter for the example above corresponds to about 11 bits.
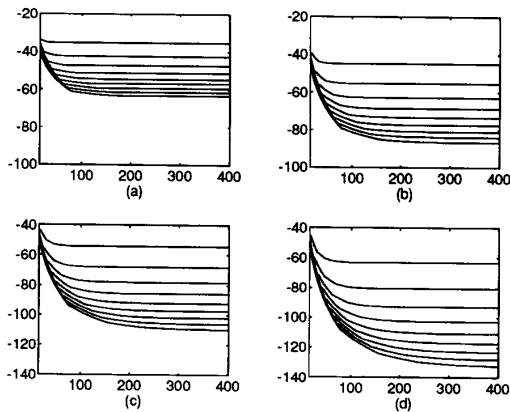
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Figure 3: The power in dB of the overall quantization error component relative to Δ^2 versus filter length, N, with M=8, 12, 16,..., 40 for (a) second-order, (b) third-order, (c) fourth-order, and (d) fifth-order $\Delta\Sigma$ modulators.

The resolution of the $\Pi\Delta\Sigma$ converter for P-order modulators is shown in Fig. 4. The filter lengths used were such that no appreciable gain in performance could be obtained by lengthening them further. In each case the curve is approximately straight and for every doubling of the number of channels, the overall quantization error power decreases by approximately $6P$ dB. Thus, the $\Pi\Delta\Sigma$ modulator gives an additional P bits for each doubling in the number of channels.

II. Design Considerations

To explore the design considerations of the $\Pi\Delta\Sigma$ A/D converter, we use the error model developed for a single channel of the converter, Fig. 5. For this example, each channel consists of a second-order modulator with a 2-level quantizer. Using this model, it is possible to evaluate the design requirements of each circuit block in a single channel to obtain the overall desired converter performance. The input signal offset is modeled by f_{xm} and the input referred offset of the integrator is described by f_m. The integrator gain errors are modeled by k and the error in the integrator pole location is modeled by p. Additionally, the offset and gain error of the DAC is modeled by t_m. Using this model it was found that the critical design considerations of a single channel modulator also apply to the $\Pi\Delta\Sigma$ modulator. Relatively large DAC offset errors have no detrimental affect on the converter performance while the DAC gain errors quickly degrade the resolution, Fig. 6. For an operational amplifier open loop gain greater than 10 the converter exhibits nearly ideal performance which is similar to the $\Delta\Sigma$ converter. The input offset error, Fig. 7, can introduce significant errors for offsets greater than $0.01(\Delta/2)$, where Δ is quantizer step size.
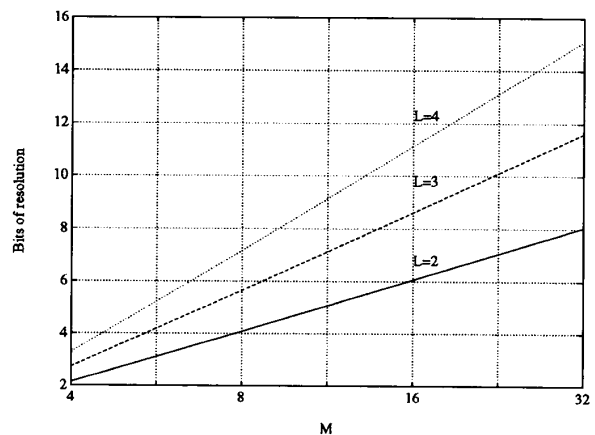
Figure 4: $\Pi\Delta\Sigma$ A/D converter resolution vs. number of channels, M.

III. Design Implementation

A $\Pi\Delta\Sigma$ modulator was constructed from second-order switched-capacitor modulators, Fig. 8. Each $\Delta\Sigma$ modulator consists of a Hadamard modulator on its input, Fig. 9. The modulator simply consists of switches which either pass the differential signal or cross the inputs. Transmission gates operating with the same clocks as the $\Delta\Sigma$ modulator are used so that no additional clock signals are required. Fully-differential folded-cascode op amps with open loop gain of 60 dB, unity gain bandwidth of 200 MHz, slew rate of 300V/μs and switched-capacitor common-mode feedback were used for the integrators in the modulators. To reduce the errors due to charge injection, transmission gates were used throughout the design.

IV. Measured Results

Five modulators were integrated onto a single 1.8mm x 1.8mm 1.2 μCMOS chip, Fig. 12. Three modulators are along the top of the photograph and two are below. In each modulator the operational amplifiers are isolated from the switches by the capacitors (above and below). In the lower left-hand corner of the die is an op amp and comparator for test purposes. The Hadamard sequence is generated off-chip and it controls the switches on-chip. This allows combining any number of parallel channels in testing the architecture. The buffered output of each modulator connects to an output pin so that filtering and demodulation may be performed to obtain the overall converter output.

To test the architecture, several chips were wired in parallel. A Tektronix LV500 digital tester was used to supply the digital Hadamard sequences and collect the output data from each channel. The full-rate 16-channel $\Pi\Delta\Sigma$ A/D converter output spectrum clocked at 1 MHz and with input

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signal of 50 kHz is shown in Fig. 10. As predicted by the theory, each doubling in the number of channels increase the resolution by 2 bits. The 16-channel converter achieved 5.7 bits of resolution. The SNR plus distortion plot versus input amplitude is shown in Fig. 11. As expected, the signal overloads at approximately -5 dB. In order to improve further on the resolution of this converter, the 16-channel $\Pi\Delta\Sigma$ modulator is next oversampled by a factor of 3. The output spectrum for this converter again clocked at 1 MHz with no input signal revealed a resolution of 8.7 bits. Further increases in the resolution requires calibration.

The data presented here is with a 1 MHz clock signal but all of the circuitry is designed to operate with a 40 MHz clock. At this time, the large loading capacitance of the tester is limiting the speed of the tests. It is anticipated that with proper buffering to the tester that clock and conversion rates of 40 MHz will be achievable. This would then allow 8.7 bits of resolution at a conversion rate of 5 MHz. Further improvements in the resolution can be obtained by increasing the oversamping rate, increasing the number of channels or using a higher order modulator on each channel.

V. Conclusion

This paper presents a new A/D architecture for obtaining high resolution data convertion using $\Delta\Sigma$ modulators without requiring oversampling. The theory has been verified through a 16-channel $\Pi\Delta\Sigma$ A/D converter implementation where both oversampling (by a factor of 3) and no oversampling were used. The combination of some oversampling and multiple channels could be very promising for many applications. Future research will be focused on implementing a high speed converter with greater than 10 bits of resolusion. From the experiments performed here it is anticipated that digital calibration will be required.

References

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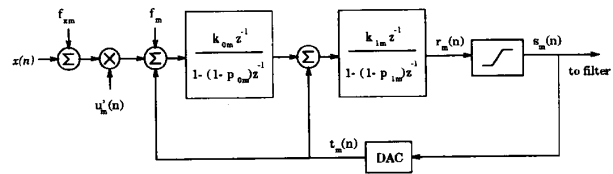
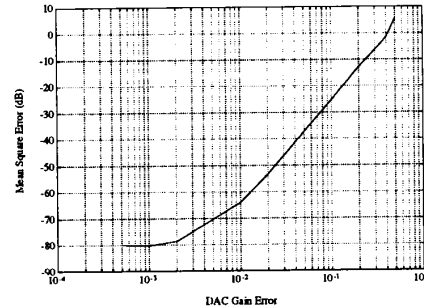Figure 5: An error model for a single channel of the $\Pi\Delta\Sigma$ A/D converter.

Figure 6: Performance degradation due to DAC gain errors in the $\Pi\Delta\Sigma$ A/D converter.
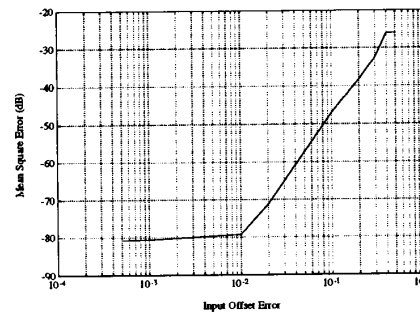

Figure 7: Performance degradation due to input offset errors in the $\Pi\Delta\Sigma$ A/D converter.
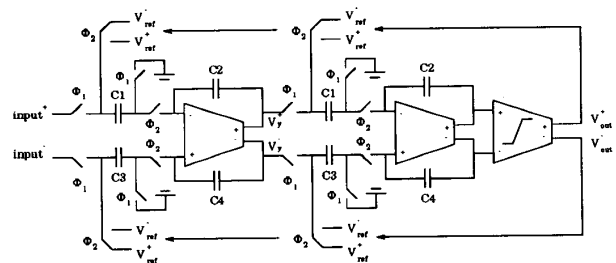

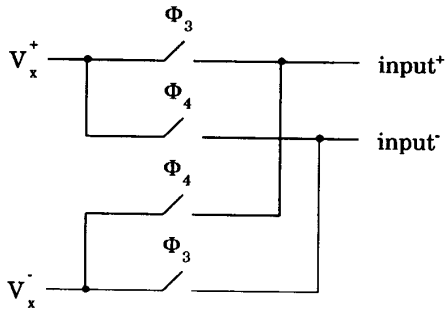Figure 8: Second-order $\Delta\Sigma$ Modulator.
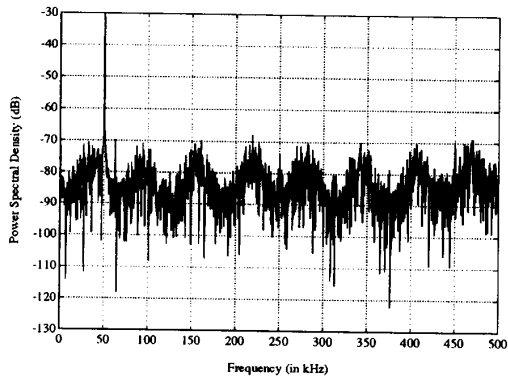
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Figure 9: Hadamard modulator.

Figure 10: Output spectrum of the full-rate (1 MHz) $\Pi\Delta\Sigma$ A/D converter implemented with 16-channels of second-order $\Delta\Sigma$ modulators.
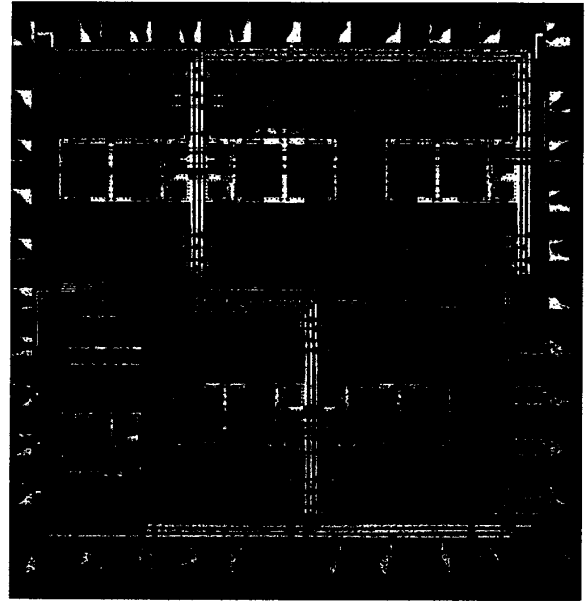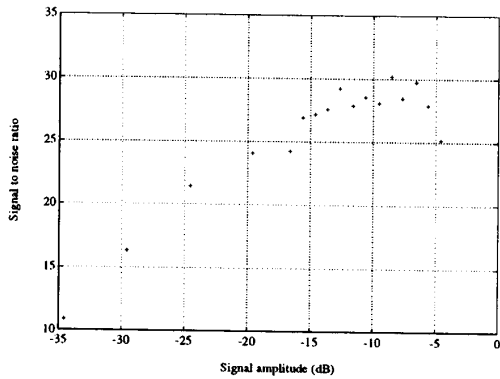

Figure 12: Die microphotograph.

Figure 11: Signal-to-(noise+distortion) ratio plot versus input amplitude (where $0dB = \Delta/2 = 2V$.

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